User's Guide

Publication number E2449-97002
February 2002

For Safety information, Warranties, and Regulatory information, see the pages behind Appendix A

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E2449B PowerPC 403GA, 601, 603, and 604 Interface Software

The E2449B Interface Software — At a Glance

The E2449B Interface Software provides a complete interface for state or timing analysis between an appropriately-designed PowerPC target system and an logic analyzer. Table 1 shows the PowerPC microprocessors and logic analyzers supported by the inverse assembler.

Table 1. Logic Analyzer Support for PowerPC Microprocessors

	403GA	601	603/603e	604/604e
1660 series	x	x	x	x
1661 series	x	--	--	--
1670 series	x	x	x	x
1671 series	x	--	--	--
16550A (one card)	x	--	--	--
16550A (two card)	x	x	x	x
16554A/55A/56A (two or three cards)	x	x	x	x
16555D/56D (two or three cards)	x	x	x	x

The configuration software on the flexible disk sets up the format specification menu of the logic analyzer for compatibility with the microprocessors. It also loads the inverse assembler for obtaining displays of PowerPC data in PowerPC assembly language mnemonics.

In This Book

This book is the user's guide for the E2449B PowerPC Interface Software. It assumes that you have a working knowledge of the logic analyzer used and the microprocessor being analyzed.

This user's guide is organized into three chapters and one appendix:

Chapter 1 explains how to install and configure the software for state or timing analysis with the supported logic analyzers.

Chapter 2 provides reference information on the format specification and symbols configured by the software and information about the inverse assemblers and status encoding.

Chapter 3 contains additional reference information including the signal mapping for the E2449B PowerPC Interface Software.

Appendix A contains information on troubleshooting problems or difficulties which may occur.

For more information on the logic analyzers or microprocessor, refer to the appropriate reference manual for those products.

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2 Analyzing the PowerPC

3 Preprocessor Interface Hardware Reference

A If You Have a Problem

1

Setting Up the PowerPC Interface Software

Setting Up the PowerPC Interface Software

This chapter explains how to install and configure the E2449B PowerPC Interface Software for state or timing analysis with the supported logic analyzers.

This section lists the logic analyzer supported by the E2449B, and provides other information about target system design and the inverse assembler.

Equipment Supplied

The E2449B Interface Software consists of the following equipment:

- The inverse assembler software and configuration files on seven 3.5-inch disks.
- 16505A Prototype Analyzer configuration files on two 3.5-inch disks (only for 603/603e and 604/604e target systems).
- This User's Guide.

Minimum Equipment Required

The minimum hardware for analysis of a 403GA, 601, 603/603e, or 604/604e target system consists of the following equipment:

- The E2449B Interface Software.
- A method for connecting to the logic analyzer (see "Connecting to the Target System").
- One of the logic analyzers listed in the following table:

Table 2. Logic Analyzers Supported

Logic Analyzer	Channel Count	State Speed	Timing Speed	Memory Depth
1660A/AS/C/CS	136	100 MHz	250 MHz	4 k states
1661A/AS/C/CS*	102	100 MHz	250 MHz	4 k states
1670A	136	70 MHz	125 MHz	64 k or 512 k
1670D	136	100 MHz	125 MHz	64 k or 1 M
1671A*	102	70 MHz	125 MHz	64 k or 512 k
1671D*	102	100 MHz	125 MHz	64 k or 1 M
16550A (one card) *	102	100 MHz	250 MHz	4 k states
16550A (two card)	204	100 MHz	250 MHz	4 k states
16554A (two card)	136	70 MHz	125 MHz	512 k states
16555A/D (two card)	136	110 MHz	250 MHz	1 M/2 M states
16556A/D (two card)	136	100 MHz	200 MHz	1 M/2 M states

* These logic analyzers only support analysis of PowerPC 403.

Connecting to the Target System

The method for connecting the logic analyzer to the target system depends on the target system design. Broadly speaking, there are four possible approaches:

- Including logic analyzer connectors on the target system
- Probing the microprocessor with a QFP (Quad Flat Pack) adapter; the pins on the QFP adapter can then be probed with the GP (General Purpose) probes supplied with the logic analyzer
- Probing the target directly with GP probes
- For target systems that contain a 190-pin L2 Cache/PDS socket, using the E2455-60002 interface socket (adapts 190-pin socket to six high-density logic analyzer connectors)

The following sections contain information on designing or using these approaches. The signal-to-connector mapping, showing which signals must go to which logic analyzer connector, are shown in chapter 3.

Designing and using built-in connectors

For the logic analyzer user, the simplest method for connecting to the logic analyzer is to have analyzer-compatible connectors designed into the target. IBM's PowerPC 403GA Evaluation Board, for example, includes eight 2x10 connectors.

The primary concerns when using built-in connectors are the board real estate required by the connectors, ensuring that the logic analyzer is properly terminated, and ensuring that the microprocessor pins connect to the proper logic analyzer probes.

A number of connector schemes are available. These schemes are described in detail on the following pages. A brief summary of these schemes is covered in the following table.

Table 3. Summary of Built-in Connectors

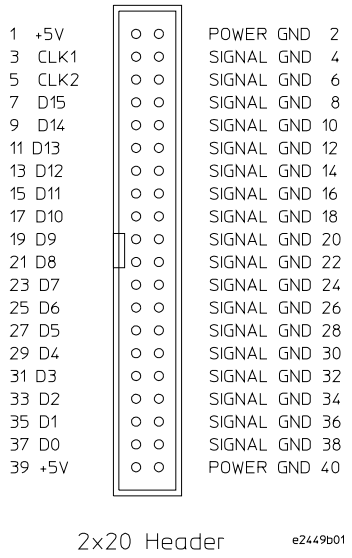
2x20 Connectors	low density requires on-board RC termination plugs directly into logic analyzer cables
2x10 Connectors	medium density requires termination adapter (part number 01650-63203) not recommended above 50 MHz
2x19 Connectors	highest density (each connector supports two logic analyzer pods) requires E5346A cables

Some of these schemes require an RC termination network on board for each probed signal. The terminations are available in SIP (single inline package), DIP (double inline package), and SMT (surface mount technology) packages. Additional information is available in Application Notes 1244-1 and 5962-8620E. A summary of the part numbers is located on page 1-10.

2x20 Headers

The 2x20 headers are low density connectors. Each connector plugs directly into a standard logic analyzer cable, and carries 16 microprocessor signals and a clock (CLK1). This connection scheme requires on-board RC termination. Figure 1 shows the pinout for a 2x20 header. Refer to chapter 3 for the tables showing the microprocessor signals for each pin. Note that the +5V pins (1 and 39) supply power from the logic analyzer to active devices on an interface board. In most instances, these pins should not be used.

Figure 1



Pinout for 2x20 header

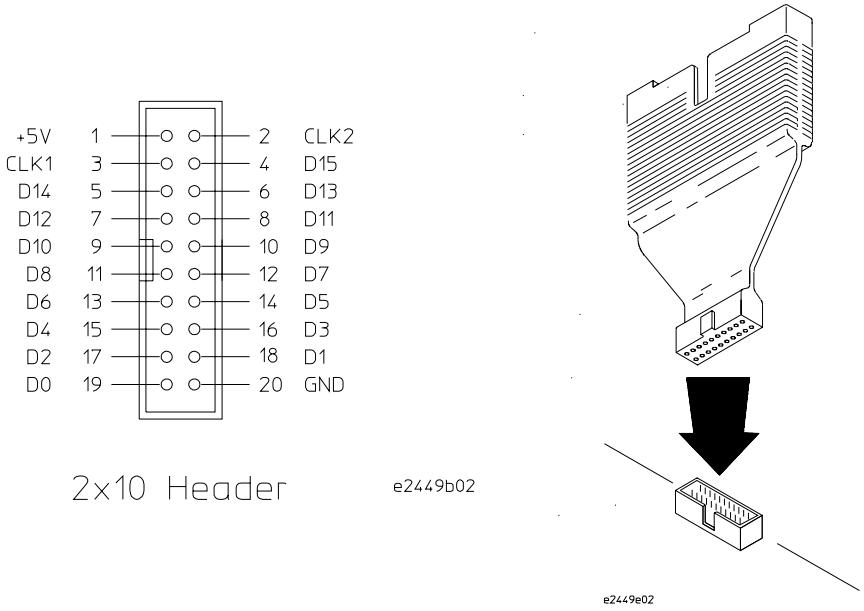
2x10 Headers

The 2x10 headers are medium density connectors. Each connector carries 16 microprocessor signals plus one clock (CLK1). This connection scheme requires one 100 kOhm Termination Adapter per connector (part number 01650-63203). On-board RC termination is not required.

Figure 2 shows the pinout for a 2x10 header. Refer to chapter 3 for the tables showing the microprocessor signals for each pin. Note that the +5V pin (pin 1) supplies power from the logic analyzer to active devices on an interface board. In most instances, this pin should not be used.

This connection scheme is not recommended for target systems operating above 50 MHz.

Figure 2



2x10 header pinouts and Termination Adapter

2x19 High-Density AMP Mictor Headers

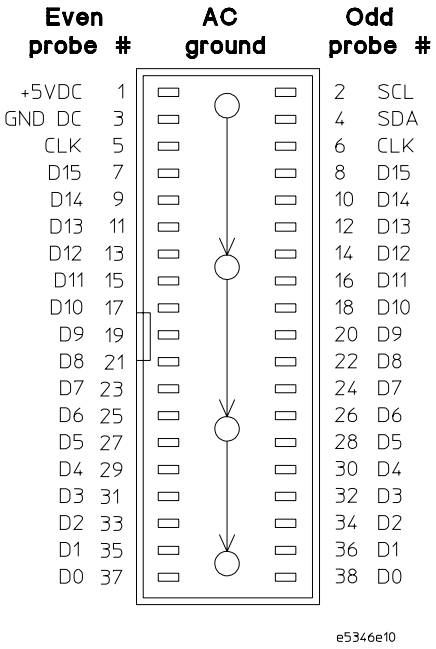
The 2x19 headers are high density connectors. Each connector carries 32 microprocessor signals plus two clocks (CLK1 for two logic analyzer pods). A special flexible cable adapter is required to connect the logic analyzer cables to the connector (part number E5346A). This cable contains the required termination. One cable adapter is required for every two logic analyzer pods.

Figure 3 shows the pinout for a 2x19 header. Refer to chapter 3 for the tables showing the microprocessor signals for each pin. Note that the +5V pin (pin 1) is used to supply power from the logic analyzer to any active devices on an interface board. In most instances, this pin should not be used.

To increase the structural support for the cables, you can also use cable supports (part number E5346-44701) on each connector.

If you use the 2x19 high-density connectors, refer to "To connect the high-density cables to the target system."

Figure 3



2x19 header pinouts

Part Numbers for Built-in Connectors

The following table contains part numbers for the components required for each connection scheme.

Table 4. Part Numbers for Built-in Connectors

	Header Part No.	On-board Termination Required	Adapter to Analyzer Cable
2x20	1251-8828	DIP 1810-1278 (9 per part) SIP 1810-1588 (5 per part)	none
2x10	1251-8106	none	01650-63203 Termination Adapter (one per analyzer pod)
2x19	1252-7431, or AMP 767-004-1. The connector support part number is E5346-44701.	none	E5346A cable (one per every two logic analyzer pods)

Direct Probing with GP Probes

If you are using GP probes, connect the individual probes to the signals according to the tables in chapter 3. It is helpful to label the probe headers before installing the probes. You should connect the ground signal for the analyzer clock(s), and two to four signal grounds per pod.

Probing with a QFP adapter

Various probing solutions are available for chips in Quad Flat Pack (QFP) packages. These are available from and various third-party vendors.

Using a Cache/PDS expansion socket

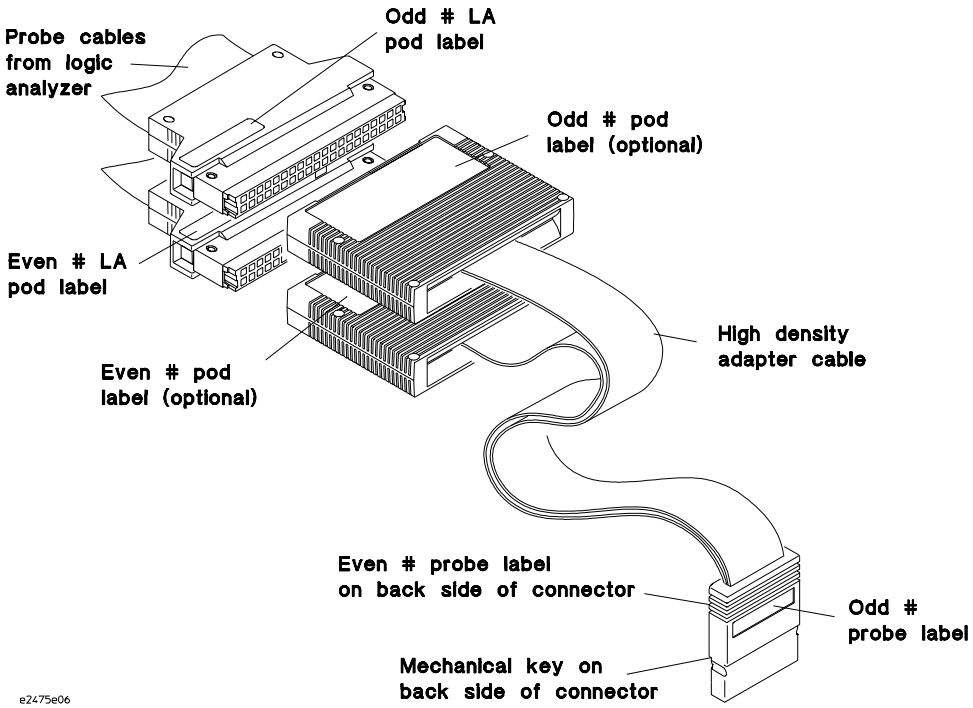
The E2455-60002 Preprocessor Interface circuit board connects directly to a 190-pin socket on a target system, and provides six connectors (2 x 19) for the high-density cables. The signals are appropriately routed from the target system to the logic analyzer for direct connection.

To connect the high-density cables to the target system

The 2x19 high-density cables include labels to identify them. The labels identify the cables by the pod number, and "o" or "e" (for odd or even). Attach the labels to the cables, then connect the cables to the connectors on the target system as shown in the illustration on the following page.

The 2x19 cables connect the signals for two logic analyzer pods. When connecting to the logic analyzer, use the tables in chapter 3 to correlate the high-density cables to the Jx or Px connector designations.

Figure 4



E5346A Cable Numbering

Connecting to the Logic Analyzer

The following sections list the connection tables for connecting the logic analyzer pods to the target system connectors or signals. Note that there are different sections for the PowerPC 403GA, 601, 603/603e, and 604/604e. The connection table used also depends on which logic analyzer is used. The configuration file for the specific logic analyzer and microprocessor is listed at the bottom of each table.

Connecting to the PowerPC 403GA

Connections to J1, J2, J3, J4, and J5 are required for inverse assembly. Connections to J6, J7, and J8 are optional.

Table 5. 1660A/AS/C/CS Connections for 403GA

1660	Pod 8	Pod 7	Pod 6	Pod 5	Pod 4	Pod 3	Pod 2	Pod 1
	J1 ADDR	J2 ADDR	J6 DMA	J8 JTAG	J3 DATA	J4 DATA	J5 STAT clk↑	J7 DRAM
Use configuration file **C403J** or **CU403J**								

Table 6. 1670A/D Connections for 403GA

1670	Pod 8	Pod 7	Pod 6	Pod 5	Pod 4	Pod 3	Pod 2	Pod 1
	J1 ADDR	J2 ADDR	J3 DATA	J4 DATA	J5 STAT clk↑	J6 DMA	J7 DRAM	J8 JTAG
Use configuration file **C403M** or **CU403M**								

Table 7. Two-card 16554/55/56 Logic Analyzer Connections for 403GA

	Pod 8	Pod 7	Pod 6	Pod 5	Pod 4	Pod 3	Pod 2	Pod 1
Expander Card					J1 ADDR	J2 ADDR	J3 DATA	J4 DATA
Master Card					J5 STAT clk↑	J6 DMA	J7 DRAM	J8 JTAG

Use configuration file **C403M** or **CU403M**

Table 8. Three-card 16554/55/56 Logic Analyzer Connections for 403GA

	Pod 8	Pod 7	Pod 6	Pod 5	Pod 4	Pod 3	Pod 2	Pod 1
Upper Expander Card					J1 ADDR	J2 ADDR	J3 DATA	J4 DATA
Master Card					J5 STAT clk↑	J6 DMA	--	--
Lower Expander Card					--	--	J7 DRAM	J8 JTAG

Use configuration file **C403M3** or **CU403M3**

Table 9. Two-card 16550A Logic Analyzer Connections for 403GA

	Pod 8	Pod 7	Pod 6	Pod 5	Pod 4	Pod 3	Pod 2	Pod 1
Expander Card			J6 DMA	J8 JTAG	J1 ADDR	J2 ADDR	J3 DATA	J4 DATA
Master Card				J5 STAT clk↑	J7 DRAM			

Use configuration file **C403F2** or **CU403F2**

Table 10. One-card 16550A Logic Analyzer, 1671A/D, and 1661A/AS/C/CS Connections for 403GA

	Pod 8	Pod 7	Pod 6	Pod 5	Pod 4	Pod 3	Pod 2	Pod 1
			J1 ADDR	J2 ADDR	J3 DATA	J4 DATA	J5 STAT clk↑	*

Use configuration file **C403F** or **CU403F**
*This logic analyzer pod can be connected to J6, J7, or J8, depending on the analysis requirements

Connecting to the PowerPC 601

Connections to P1, P2, P3, P4, P5, P6, P7, and P8 are required for inverse assembly. Connections to P9 and P10 are optional.

Table 11. Two-card 16554/55/56 Logic Analyzer Connections for 601

	Pod 8	Pod 7	Pod 6	Pod 5	Pod 4	Pod 3	Pod 2	Pod 1
Expander Card					P8 STAT	P7 STAT	P2 ADDR	P1 ADDR
Master Card					P6 DATA	P5 DATA	P4 DATA_B	P3 DATA_B clk↑

Use configuration file **C601M** or **CP601M**

Table 12. 1670A/D Logic Analyzer Connections for 601

1670	Pod 8	Pod 7	Pod 6	Pod 5	Pod 4	Pod 3	Pod 2	Pod 1
	P8 STAT	P7 STAT	P2 ADDR	P1 ADDR	P6 DATA	P5 DATA	P4 DATA_B	P3 DATA_B clk↑

Use configuration file **C601M** or **CP601M**

Table 13. Three-card 16554/55/56 Logic Analyzer Connections for 601

	Pod 8	Pod 7	Pod 6	Pod 5	Pod 4	Pod 3	Pod 2	Pod 1
Upper Expander Card					P8 STAT	P7 STAT	P2 ADDR	P1 ADDR
Master Card					P4 DATA_B	P3 DATA_B clk↑		
Lower Expander Card					P10 misc	P9 PARITY	P6 DATA	P5 DATA

Use configuration file **C601M3** or **CP601M3**

Table 14. Two-card 16550A Logic Analyzer Connections for 601

	Pod 8	Pod 7	Pod 6	Pod 5	Pod 4	Pod 3	Pod 2	Pod 1
Expander Card			P10 misc	P9 PARITY	P8 STAT	P7 STAT	P6 DATA	P5 DATA
Master Card			P4 DATA_B	P3 DATA_B clk↑	P2 ADDR	P1 ADDR		

Use configuration file **C601F** or **CP601F**

Table 15. 1660A/AS/C/CS Logic Analyzer Connections for 601

1660	Pod 8	Pod 7	Pod 6	Pod 5	Pod 4	Pod 3	Pod 2	Pod 1
	P8 STAT	P7 STAT	P6 DATA	P5 DATA	P4 DATA_B	P3 DATA_B clk↑	P2 ADDR	P1 ADDR

Use configuration file **C601J** or **CP601J**

Connecting to the PowerPC 603/603e

Connections to J2, J3, J4, J5, J7, J8, J9, and J10 are required for inverse assembly. Connections to J1 and J6 are optional.

Table 16. Two-card 16554/55/56 Logic Analyzer Connections for 603/603e

	Pod 8	Pod 7	Pod 6	Pod 5	Pod 4	Pod 3	Pod 2	Pod 1
Expander Card					J9 DATA	J7 DATA	J10 DATA_B	J8 DATA_B
Master Card					J5 STAT	J2 STAT	J3 ADDR	J4 ADDR clk↑

Use configuration file **C603M** or **CP603M**

Table 17. Three-card 16554/55/56 Logic Analyzer Connections for 603/603e

	Pod 8	Pod 7	Pod 6	Pod 5	Pod 4	Pod 3	Pod 2	Pod 1
Upper Expander Card					J9 DATA	J7 DATA	J10 DATA_B	J8 DATA_B
Master Card					J6 misc	J1 misc	J3 ADDR	J4 ADDR clk↑
Lower Expander Card							J5 STAT	J2 STAT

Use configuration file **C603M3** or **CP603M**3

Table 18. Two-card 16550A Logic Analyzer Connections for 603/603e

	Pod 8	Pod 7	Pod 6	Pod 5	Pod 4	Pod 3	Pod 2	Pod 1
Expander Card			J5 STAT	J2 STAT	J9 DATA	J7 DATA	J10 DATA_B	J8 DATA_B
Master Card			J6 misc	J1 misc	J3 ADDR	J4 ADDR clk↑		

Use configuration file **C603F** or **CP603F**

Table 19. 1660A/AS/C/CS Logic Analyzer Connections for 603/603e

1660	Pod 8	Pod 7	Pod 6	Pod 5	Pod 4	Pod 3	Pod 2	Pod 1
	J5 STAT	J2 STAT	J9 DATA	J7 DATA	J10 DATA_B	J8 DATA_B	J3 ADDR	J4 ADDR clk↑

Use configuration file **C603J** or **CP603J**

Table 20. 1670A/D Logic Analyzer Connections for 603/603e

1670	Pod 8	Pod 7	Pod 6	Pod 5	Pod 4	Pod 3	Pod 2	Pod 1
	J9 DATA	J7 DATA	J10 DATA_B	J8 DATA_B	J5 STAT	J2 STAT	J3 ADDR	J4 ADDR clk↑

Use configuration file **C603M** or **CP603M**

Connecting to the PowerPC 604/604e

Connections to P2, P3, P4, P5, P7, P8, P9, and P10 are required for inverse assembly. Connections to P1, P6, and P11 are optional.

P11, the "cache" pod, contains PDS/L2-cache signals which are not processor bound. Typically, these are signals on an MPC105 Cache/Memory controller chip.

Table 21. Two-card 16550A Logic Analyzer Connections for 604/604e

	Pod 8	Pod 7	Pod 6	Pod 5	Pod 4	Pod 3	Pod 2	Pod 1
Expander Card			P5 STAT	P2 STAT	P10 DATA	P8 DATA	P9 DATA_B	P7 DATA_B
Master Card			P1 misc	P6 misc	P4 ADDR	P3 ADDR clk↑	P11 cache	--

Use configuration file **C60XF**

Table 22. 1660A/AS/C/CS Logic Analyzer Connections for 603/603e

1660	Pod 8	Pod 7	Pod 6	Pod 5	Pod 4	Pod 3	Pod 2	Pod 1
	P10 DATA	P8 DATA	P9 DATA_B	P7 DATA_B	P5 STAT	P2 STAT	P4 ADDR	P3 ADDR clk↑

Use configuration file **C60XJ**

Table 23. 1670A/D Logic Analyzer Connections for 603/603e

1670	Pod 8	Pod 7	Pod 6	Pod 5	Pod 4	Pod 3	Pod 2	Pod 1
	P10 DATA	P8 DATA	P9 DATA_B	P7 DATA_B	P5 STAT	P2 STAT	P4 ADDR	P3 ADDR clk↑

Use configuration file **C60XM**

Table 24. Two-card 16554/55/56 Logic Analyzer Connections for 604/604e

	Pod 8	Pod 7	Pod 6	Pod 5	Pod 4	Pod 3	Pod 2	Pod 1
Expander Card					P10 DATA	P8 DATA	P9 DATA_B	P7 DATA_B
Master Card					P5 STAT	P2 STAT	P4 ADDR	P3 ADDR clk↑

Use configuration file **C60XM**

Table 25. Three-card 16554/55/56 Logic Analyzer Connections for 604/604e

	Pod 8	Pod 7	Pod 6	Pod 5	Pod 4	Pod 3	Pod 2	Pod 1
Upper Expander Card					P10 DATA	P8 DATA	P9 DATA_B	P7 DATA_B
Master Card					P5 STAT	P2 STAT	P4 ADDR	P3 ADDR clk↑
Lower Expander Card					P1 misc	P6 misc	P11 cache	--

Use configuration file **C60XM3**

Setting Up the Inverse Assembler Software

Setting up for the inverse assembler software consists of the following major steps:

1. **The first time you set up the inverse assembler, make a duplicate copy of the master disk.**

   For information on duplicating disks, refer to the reference manual for your logic analyzer.

2. **Select the proper E2449B disk and insert it in the front disk drive of the logic analyzer.**

3. **Load the appropriate configuration file into the logic analyzer.**

   Once you have the hardware and software set up, you are ready to make measurements with the logic analyzer and inverse assembler. The rest of this section provides more detailed information on setting up the logic analyzer software.

To load the configuration and inverse assembler files

1. **Select the proper E2449B disk and insert it in the front disk drive of the logic analyzer.**

   There are seven logic analyzer disks and two prototype analyzer disks supplied with the E2449B. The seven logic analyzer disks correspond to the columns in the table on the next page.

2. **Depending on your logic analyzer, select one of the following menus:**

   - For the 1660-series logic analyzers, select the "System Disk" menu
   - For the 16500A mainframe, select the "System Front Disk" menu
   - For the 16500B/C mainframe, select the "System Flexible Disk" menu

3. **Configure the menu to "Load" the analyzer configuration from disk.**
4. **Select the appropriate module (such as "100/500 MHz LA" or "Analyzer") for the load.**
5. **Use the knob to select the appropriate configuration file.**

   Your configuration file choice depends on which analyzer you are using and the type of measurements you want to make. The configuration file names are located at the bottom of the table showing the connections for your particular microprocessor and logic analyzer. The next section describes the differences between the configuration files.

6. **Execute the load operation to load the file into the logic analyzer.**

   The logic analyzer is configured for PowerPC analysis by loading the appropriate PowerPC configuration file. Loading this file also automatically loads an inverse assembler. For PowerPC 603/603e and PowerPC 604/604e target systems, there are two different inverse assemblers, described in chapter 2.

7. If you want to load a different inverse assembler, repeat steps 2 through 6, selecting the inverse assembler file in step 4. Refer to "Using the Inverse Assembler" in Chapter 2 for information on inverse assemblers.
8. **If you are using the 16505A Prototype Analyzer, insert the "16505 Prototype Analyzer" flexible disk into the disk drive of the prototype analyzer and update the 16505A from the Session Manager. You must close your workspace to run the update.**

   The 16505A Prototype Analyzer requires software version A.01.22 or higher to work with the E2449B. Only the 603/603e and 604/604e are supported.

To select the proper configuration file

For the PowerPC 403, 601, and 603/603e, there are two configuration files for each analyzer. The PowerPC 604/604e has one configuration file for each analyzer.

For the PowerPC 601 and 603/603e, there is one configuration file for AACK-before-TA (pipelined) systems, and one configuration file for AACK-delayed-until-last-TA (non-pipelined) systems. The only difference in the configuration files is the inverse assembler attached: one looks backwards from TA for AACK, the other looks forward.

For the PowerPC 403GA, there is one configuration file for systems that have IOTV (input/output transaction valid) enabled, and one for systems that have IOTV disabled. IOTV is used as a storage qualification term; in its absence, the logic analyzer uses state-per-clock capture, and the amount of information captured by the logic analyzer is reduced. The procedure for enabling IOTV is located on page 2-8.

Table 26 summarizes the configuration files:

Table 26. Configuration Files

analyzer	403 IOTV	403 st/clk	601 piped	601 non-pipe	603/603e piped	603/603e non-pipe	604/604e
2-card 16554/5/6	C403M	CU403M	CP601M	C601M	CP603M	C603M	C60XM
3-card 16554/5/6	C403M3	CU403M3	CP601M3	C601M3	CP603M3	C603M3	C60XM3
2-card 16550	C403F2	CU403F2	CP601F	C601F	CP603F	C603F	C60XF
1-card 16550	C403F	CU403F	--		--		--
1660	C403J	CU403J	CP601J	C601J	CP603J	C603J	C60XJ
1661	C403F	CU403F	--		--		--
1670	C403M	CU403M	CP601M	C601M	CP603M	C603M	C60XM
1671	C403F	CU403F	--		--		--

To set up the analyzer for timing

The same format specification loaded for state analysis is also used for timing analysis. To configure the logic analyzer for timing analysis:

1. Select the Configuration menu of the logic analyzer.
2. Select the Type field for the analyzer and select Timing.

2

Analyzing the PowerPC

Analyzing the PowerPC

This chapter describes how to display configuration information, gives status information label and symbol encodings, and provides information about the available inverse assemblers.

Displaying Information

This section describes how to display analyzer configuration information, state and timing data captured by the preprocessor interface, and symbol information that has been set up by the preprocessor interface configuration software.

The HP logic analyzers and the PowerPC use opposite conventions to designate individual signals on a bus. In PowerPC nomenclature, bit 0 is the most significant; in the logic analyzers, bit 0 is the least significant. In PowerPC, A0 is the most significant bit of the address bus; on the analyzer, this bit is called ADDR31.

Most Significant	Least Significant	
A0	A31	PowerPC
ADDR31	ADDR0	Analyzer

This may cause confusion in the waveform menus when using Channel Mode Sequential or Individual.

To display the format specification

- **Select the format specification menu for your logic analyzer.**

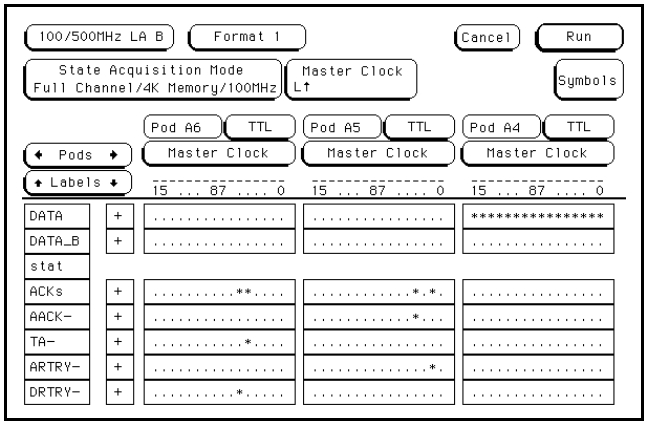
  The PowerPC configuration files contain predefined format specifications. These format specifications include all labels for monitoring the microprocessor.

  Chapter 3 of this guide contains a table that lists the signals for the PowerPC microprocessors and on which pod and probe line the signal comes to the logic analyzer. Refer to this table and to the logic analyzer connection information for your analyzer in chapter 1 to determine where the microprocessor signals should be on the format specification screen.

Example

The format specification display shown in the following figure is from the PowerPC 603 HP 16550A logic analyzer configuration. Additional labels and pod assignments are listed off the screen. Select the "Labels" field and rotate the knob on the analyzer front panel to view additional signals. Select the "Pods" field and rotate the knob to view other pod-bit assignments. There may be some slight differences in the display shown by your particular analyzer.

Figure 5



Format Listing

To display the symbols

- **Select the "Symbols" field on the format specification menu and then choose a label name from the "Label" pop-up. The logic analyzer will display the symbols associated with the label.**

  The HP E2449B configuration software sets up symbol tables on the logic analyzers. The tables contain alphanumeric symbols which identify data patterns or ranges. Labels have been defined in the format specification menu to make triggering on specific PowerPC cycles easier. The label base in the symbols menu is set to hexadecimal to conserve space in the listing menu.

  The following tables describe the PowerPC status signals and list the label and symbol encodings defined by the logic analyzer configuration software. There are separate tables for the 403GA, 601, 603/603e, and 604/604e.

Table 27. Symbol Description for PowerPC 403GA (IOTV only)

Label	Symbol	403GA Encoding
STAT	pgm	xx xxxx xxxx xxxx 1xxx x111
	rd data	xx xxxx xxxx xxxx 1xxx x101
	wr data	xx xxxx xxxx xxxx 0xxx x111
	data	xx xxxx xxxx xxxx xxxx x111
	IOTV	xx xxxx xxxx xxxx xxxx xxx1
R/-W	rd	1
	wr	0
IOTV	(blank)	0
	valid transfer	1
ERROR	(blank)	0
	error	1
BusErr	bus error	0
	(blank)	1

Table 28. Symbol Description for PowerPC 601, 603/603e, and 604/604e

Label	Symbol	601 Encoding	603/603e Encoding	604/604e Encoding
ACKs	idle	1111	1111	1111
	ARTRY	x0xx	xxx0	xxx0
	DRTRY	xxx0	0xxx	0xxx
	TA AACK	0x0x	x00x	x00x
	AACK	0xxx	xx0x	xx0x
	TA	xx0x	x0xx	x0xx
R/-W	rd	1	1	1
	wr	0	0	0

(continued)

Label	Symbol	601 Encoding	603/603e Encoding	604/604e Encoding
TSIZ	burst	0xxx	xxx0	xxx0
	8 byte	1000	0001	0001
	1 byte	1001	0011	0011
	2 byte	1010	0101	0101
	3 byte	1011	0111	0111
	4 byte	1100	1001	1001
	5 byte	1101	1011	1011
	6 byte	1110	1101	1101
	7 byte	1111	1111	1111
TT	Kill Block	0110x	0110	01100
	Wr Graphics	1010x	1010	10100
	Rd Graphics	1110x	1110	11100
	Clean Block	0000x	0000	00000
	Write	0001x	0001	00010
	Wr/Kill	0011x	0011	00110
	Read	0101x	0101	01010
	Rd/Flush	0111x	0111	01110
	Wr/Atomic Flush	1001x	1001	
	STWCX			10010
	Read Atomic	1101x	1101	
	LWARX cach inhib			11010
	Rd/Flush Atomic	1111x	1111	
	LWARX miss			11110
	Flush Block	0010x	0010	00100
	DSYNC	0100x	0100	
	SYNC			01000
	LWARX hit			00001
	TLBSYNC			10010
	eieio	1000x	1000	10000
	TLB Invalidate	1100x	1100	11000

The TSIZ label includes the TBST- signal, which qualifies TSIZ.

Some transfer type (TT) and size (TSIZ) combinations are defined by the PowerPC architecture, but not asserted by the PowerPC implementations. The symbols for these combinations include a "?".

The only symbol defined for the STAT label is "inst fetch". An instruction fetch is indicated by AACK asserted (address and qualifiers valid), R/-W (TT1) asserted for read, and TC0 asserted.

603e Analysis

If you are probing a 603e, the signal labeled XATS- is actually CSE1 (and CSE, on pod J6, is actually CSE0). You may wish to change the name of this label. In the format menu, select the XATS label, and use the Modify Label feature to change the name to CSE1. (DO NOT modify the bit assignments to the STAT label.)

Trigger Menu

This section describes some PowerPC considerations in triggering the analyzer. The trigger menu determines what will be acquired by the analyzer and when it will be acquired. The HP E2449B software preconfigures a storage qualification term to exclude wait and idle states from the analyzer's memory.

To use the trigger menu for the PowerPC 403GA

The power-up default on the 403GA has the Real-Time Debug Mode (RDM) bits in the Input/Output Control Register (IOCR) cleared, so that Trace Status outputs (TS 0:6) are disabled. In this condition there are no status signals to indicate when the address and data busses are valid.

A state-per-clock configuration file is provided for this case, along with a state-per-clock inverse assembler, which infers valid states from changes in the address bus and Write Byte Enable signals. The following code sequence will configure the RDM bits in the IOCR to Bus Status mode (%01):

```
mfdcr   r10,IOCR
rlwinm  r10,r10,0,29,26         # clear bits 27 28
ori     r10,r10,8               # set bit 28
mtdcr   IOCR,r10
```

In this mode, the lower TS bits are assigned the following functions:

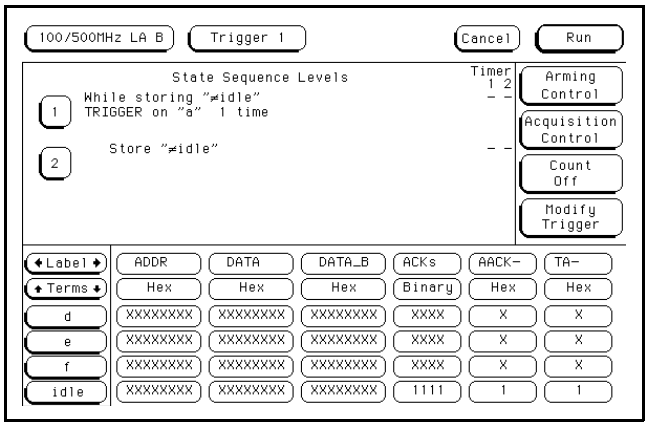
TS 0	IOTV	Input Output Transaction Valid
TS 1	I/-D	Instruction 1, Data 0
TS 2	-DMA	Processor Cycle 1, DMA Cycle 0
TS 3	BTS	Bus Transfer Start

An IOTV-aware configuration and disassembler are provided for this case. The trigger specification uses storage qualification to store only states in which IOTV is asserted.

To use the trigger menu for the PowerPC 60x

The figure below shows the trigger menu for the PowerPC 603, as configured by the HP 16550A Logic Analyzer. The configuration software renames a pattern term to "idle" and assigns it a pattern with AACK, ARTRY, TA, and DRTRY, all high (de-asserted). The sequencer is programmed to store only states "≠ idle". That is, only states where one or more of these signals is asserted will be stored.

Figure 6



Trigger Menu for PowerPC 603

To configure the analyzer to store wait and idle states, change the storage qualification from "≠ idle" to "anystate". Doing so will capture all states (state-per-clock).

To accurately trigger on a specific address, enter the address in the ADDR field of a trigger term and also enter 0 in the AACK field of the term. This will ensure against false triggering on a floating address bus.

Since the PowerPC 60x enjoy an eight byte wide data bus, instruction address will always end in hex 0 or hex 8.

When bursting, the 601 will present a quadword aligned address, which will always end in hex 0. The 603/603e and 604/604e present doubleword aligned addresses, which will end in hex 0 or hex 8. A burst consists of four double words, or 32 bytes. To accurately trigger on the fetch of a particular instruction address when bursting, the least significant five bits of the address should be "don't cares". You need to change the base of the ADDR label to binary to enter the five x's.

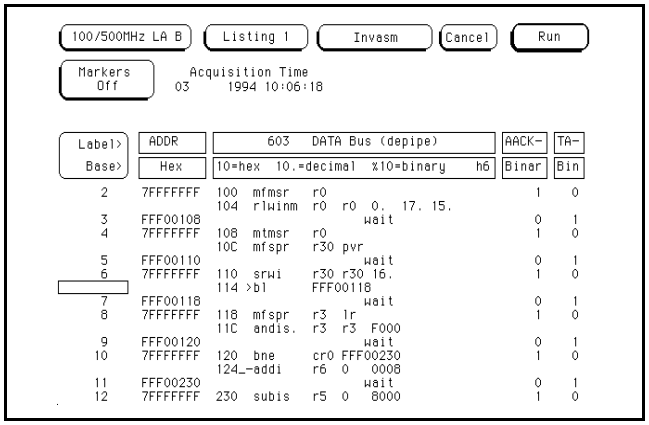
This section discusses the general output format of the inverse assemblers and microprocessor-specific information. Unless noted otherwise, the information covers all supported microprocessors.

To display captured state data

- Select the Listing Menu for your logic analyzer.

The logic analyzer displays captured data in the Listing Menu. The inverse assembler display is obtained by setting the base for the DATA label to Invasm. Figure 7 shows the Listing Menu as configured on the HP 16550A.

Figure 7



Listing Menu as configured on the HP 16550A

For the PowerPC 60x, the columns on the left of the inverse assembler display are the least significant hexadecimal digits of an instruction or burst address. These may be useful for matching an execution trace to an assembly listing. Because the PowerPC 60x present one address and then read two or eight instruction for each address, the low-order bits are synthesized by the disassembler. The actual address bits presented by the 60x may be observed under the ADDR label.

Since the 403GA presents an address for each instruction fetched from the bus, this information is not duplicated for the 403GA inverse assembler.

The next column may contain an underscore "_", which indicates a break in the sequential flow of instruction addresses.

The next column displays overfetch and branch-and-link indicators as described in the overfetch marking section on page 2-13. The remaining disassembly listing resembles an assembly listing.

Interpreting Data

General purpose registers are displayed as r0, r1, r2, ..., r31. Floating point registers are displayed as f0, f1, ..., f31. Condition registers are displayed as cr0, cr1, ..., cr7. Special purpose and device control registers are displayed using their mnemonic.

Most numerical data is displayed in hexadecimal, e.g., "lwz r28 0044(r1)".

Bit numbers and shift counts are displayed in decimal with a dot suffix, e.g., "cror 31. 31. 31.".

A few instructions display their operands in binary with a % prefix, e.g., "mtcrf %001100000 r7".

The disassemblers decode the full PowerPC instruction set architecture, including 64-bit mode instructions and optional instructions not implemented on the various microprocessors. When these unimplemented opcodes are encountered, the instruction mnemonic has a "?" prefix. If a reserved bit is set in an instruction opcode field, a "?" is appended to the mnemonic, or in some cases to an operand.

An instruction word of 0000 0000 is decoded as "illegal". Otherwise, if an opcode is not valid, it is shown as "Undefined Opcode".

Branch instruction

If the address of a branch relative instruction is known, its target is presented as an absolute hex address (or as a symbol if it matches an ADDR pattern or range symbol). If the address of a branch relative instruction is not known, its target is displayed as a hexadecimal offset such as +00000C30 or -00000048.

If a branch hint is encoded, a "+" (for predicted taken) or a minus "-" (for predicted not taken) is appended to the conditional branch mnemonic.

Extended mnemonics

PowerPC assemblers support a number of extended mnemonics for some popular assembly language instructions. The HP E2449B disassembler supports the following dialect:

- Conditional traps and branches decode the condition mnemonically when possible. For some conditions which have no conventional mnemonics (for example, "signed less than or unsigned greater than"), the condition field is displayed in binary.
- The L bit is omitted as a compare operand. Instead, compares are decoded as "cmpw" (or "?cmpd").
- "Add immediate" instructions with a negative immediate operand are decoded as subtract immediate ("subi").
- "Subtract from" instructions "subf" and "subfc" are decoded as subtract instructions sub and subc with the source operands exchanged so that "sub r3 r4 r5" is mnemonically interpreted as "r3 = r4 - r5".
- ori r0 r0 0000 is decoded as "nop".

The following listing shows the extended mnemonics for the integer rotate instructions.

Mnemonic	Decoded As	
rlwimi (rotate left word immediate then mask insert)	inslwi	insert from left immediate
	insrwi	insert from right immediate
rlwinm (rotate left word immediate then AND with mask)	rotlwi	rotate left immediate
	rotrwi	rotate right immediate
	slwi	shift left immediate
	srwi	shift right immediate
	extlwi	extract and left justify immediate
	extrwi	extract and right justify immediate
	clrlwi	clear left immediate
	clrrwi	clear right immediate
	clrlslwi	clear left and shift left immediate
rlwnm (rotate left word then AND with mask)	rotlw	rotate left

Additional extended mnemonics for PowerPC 603/603e and 604/604e

The PowerPC 603/603e and 604/604e also support the following extended mnemonics.

- add immediate and add immediate shifted instructions, addi and addis, with a null source register are decoded as load immediate and load immediate shifted, li and lis.
- or instructions with identical source registers are decoded as move register, mr.
- nor instructions with identical source registers are decoded as not register, not.
- xor and eqv instructions with identical source and destination registers are decoded as clear and set, clr and set, respectively.
- the cror, crnor, crxor, and creqv instructions map analogously to crmv, crnot, crclr, and crset.
- when the mtcrf instruction field mask specifies the entire cr, it is decoded as mtcr.

Overfetch Marking

Overfetch refers to instructions that are are fetched but not executed by the microprocessor. They may arise from the following sources:

- When bursting, the 601 first fetches the critical quadword of an eight-word cache line; the 603/603e and 604/604e first fetch the critical doubleword; the 403GA fetches the critical word. The memory system then provides succeeding doublewords (single words for the 403GA). If the critical word was not the first quad- or double- or single word of the line, the memory system wraps at the line boundary to the first word. Fetches after the line wrap are not in the sequential execution path and are marked with an asterisk "*".
- When the microprocessors execute a branch instruction, the instructions between the branch and the branch target are not executed. These instructions are indicated with a hyphen "-". If the instruction cache is enabled, the branch target may already be in the cache and will not be fetched over the bus. The remaining cache line containing the branch will be marked as overfetch.
  In some cases, bus activity may be ambigous with regard to whether a branch is taken. In these cases, a question mark "?" is used to indicate states that may or may not have been executed.

An exception to the above includes branches with the link bit set that record the next instruction address in the link register ("lr"). Frequently, these are subroutine branches which will return to the instructions following the branch. These branch-and-link instructions may be indicated by a ">".

For conditional branches whose target addresses are not known or are known but not seen in the bus traffic, the inverse assembler cannot always determine if the branch was taken and will not mark ensuing states as overfetch.

Disabling the Instruction Cache

When the instruction cache is enabled, many PowerPC instructions may be executed from cache and will not appear on the external bus. To get an execution trace on the bus, the instruction cache can be disabled. This must be done in supervisor mode.

Disabling the Cache (403) The cacheability of areas of 403 memory space is controlled by bits in the Instruction Cache Control Register (ICCR)with a 128 megabyte granularity. For example, to disable the instruction cache for addresses 78000000 through 7FFFFFFF, the following code sequence could be used:

```
mfdcr   r1,ICCR
rlwinm  r1,r1,0,16,14 #   clear bit 15
mtdcr   ICCR,r1     #     disable i cache 78000000..7FFFFFFF
```

Disabling the Cache (601) On the 601, caching is inhibited by setting the I bit in the page table entries and Block Address Translation(BAT) registers. Refer to the 601 documentation for additional information.

Disabling the Cache (603/603e and 604/604e) On the 603/603e and 604/604e, a single bit in Hardware Implementation Dependent register 0 (HID0) globally controls instruction cacheability.

Disable the cache with the following code:

```
mfspr       r3      hid0
rlwinm      r3      r3 0 17 15          #clear bit 16(ICE)
mtspr       hid0    r3
```

- To also disable the data cache use:

```
mfspr     r3      hid0
rlwinm    r3      r3 0 18 15      #clear ICE and DCE
mtspr     hid0    r3
isync
```

- To invalidate and disable the cache use:

```
mfspr     r3      hid0
rlwinm    r3      r3 0 18 15      #clear ICE and DCE
ori       r3      0C00            # set ICFI and DCFI
mtspr     hid0    r3
sync
rlwinm    r3      r3 0 22 19      #clear ICFI and DCFI
mtspr     hid0    r3
isync
```

To use the Invasm key

The disassembler may occasionally mispredict a conditional branch instruction as taken and incorrectly mark subsequent states as overfetch. The following steps may be taken to correct this:

- Roll the first incorrectly marked state to the top of the listing screen and select the Invasm key.
- Select High or Low as the first or second word of the double word that is incorrectly marked.

Note that the PowerPC 60x may branch to the second word of a doubleword without the disassembler detecting it. This could be a branch from cache, or via the lr, ctr, or srr0 registers. If the first word of the target doubleword is a branch, the inverse assembler may incorrectly mark the subsequent word(s) as overfetch.

To use the Invasm Options key (603/603e and 604/604e)

The software for the PowerPC 603/603e and 604/604e includes enhanced inverse assemblers, which are automatically loaded on most logic analyzers. The enhanced inverse assembler contains additional features which use the increased capabilities of these logic analyzers. These features are accessed through the Invasm Options menu. Note that all the features in the other inverse assembler are included in the enhanced inverse assembler (see previous sections). The enhanced inverse assembler file has an "E" suffix.

The Inverse Assembly Options menu contains three functions: display filtering with Show/Suppress selections, Code Synchronization, and Display Options. The following sections describe these functions.

If the X or O pattern markers are turned on, and the designated pattern is found in a state that has been Suppressed with display filtering, the following message will appear on the logic analyzer display: "X (or O) pattern found, but state is suppressed."

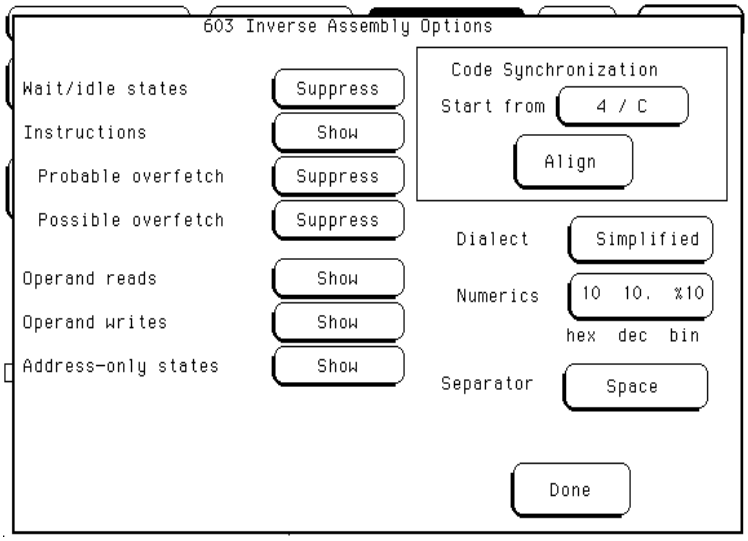
Code Synchronization

Code synchronization performs the functions of the Invasm key, previously discussed. The "0/8" selection is the high word, and "4/C" is the low word. Once you have made your selection, use the Align key to perform the operation.

Show/Suppress

The enhanced inverse assembler supports selective suppression of certain states in the state listing display. The show/suppress settings do not affect the data that is stored by the logic analyzer; they only affect whether that data is displayed or not. The same data can be examined with different settings, for different analysis requirements. The figure below shows the states that have the Show/Suppress option.

Figure 8



Suppressing wait/idle states is useful for obtaining a state-per-cycle display of acquired data. Suppressing overfetched instructions may assist in following program execution trace more clearly. Suppressing instructions may be useful if your primary interest is data operand reads and writes.

"Probable overfetch" means states marked with a "*" or "-". "Possible overfetch" means states marked with a "?".

When instructions are suppressed, the overfetch show/suppress controls have no effect.

This function allows faster analysis in two ways. First, unneeded information can be filtered out of the display. Second, particular operations can be isolated by suppressing all other operations. For example, memory writes can be shown, with all other operations suppressed, allowing quick analysis of memory writes.

Display Formats

The enhanced inverse assembler allows you to configure various aspects of the disassembler display. The configuration options are listed below.

+ Separator Either blanks or commas may be used to separate operands.

```
andis.  r3  r3  F000
andis.  r3,r3,F000
```

The generic disassemblers always use blanks as separators.

+ Numerics Either of two conventions may be selected to display numeric data. The conventions are dense and common.

	dense	common
hex	FFF00230	0xFFF00230
decimal	31.	31
binary	%00100	0b00100

Since most of the numeric data produced by the inverse assembler is hexadecimal, the dense format uses a little less screen space. The generic disassemblers always use dense numerics.

+ Dialect Three mnemonic dialects are available: Raw, Simplified, and Extended. The generic disassemblers always use the Extended dialect. The following is a list of dialect-sensitive instructions.

raw	simplified	extended
bc %00100,2,FFF00230	bne cr0,FFF00230	bne cr0,FFF00230
tw %10000,r5,r6	tw lt,r5,r6	tw lt,r5,r6
cmp cr1,0,r0,r16	cmpw cr1,r0,r16	cmpw cr1,r0,r16
ori r0,r0,0000	nop	nop
addi r6,r6,FCFC	subi r6,r6,0304	subi r6,r6,0304
subf r7,r19,r16	sub r7,r16,r19	sub r7,r16,r19
addi r3,0,7000	li r3,7000	li r3,7000
addis r3,0,7000	lis r3,7000	lis r3,7000
mtcrf %11111111,r5	mtcr r5	mtcr r5
or r4,r5,r5	mr r4,r5	mr r4,r5
nor r4,r5,r5	not r4,r5	not r4,r5
xor r7,r7,r7	clr r7	clr r7
eqv r8,r8,r8	set r8	set r8
creqv 7,7,7	crset 7	crset 7

crxor 8,8,8	crclr 8	crclr 8
cror 7,8,8	crmv 7,8	crmv 7,8
crnor 8,9,9	crnot 8,9	crnot 8,9
rlwnm r8,r7,r6,0,31.	rlwnm r8,r7,r6,FFFFFFFF	rotlw r8,r7,r6
rlwimi r3,r3,24.,8,23.	rlwimi r3,r3,24.,00FFFF00	inslwi r3,r3,16.,8
rlwimi r8,r3,17,8,23.	rlwimi r3,r3,17.,00FE0000	insrwi r8,r3,7,8
rlwinm r6,r4,8,0,14	rlwinm r6,r4,8,0xFFFE0000	extlwi r6,r4,15,8
rlwinm r6,r4,16,24,31	rlwinm r6,r4,16,0x000000FF	extrwi r6,r4,8,8
rlwinm. r6,r4,4,0,31	rlwinm. r6,r4,4,0xFFFFFFFF	rotlwi. r6,r4,4
rlwinm r6,r4,28,0,31	rlwinm r6,r4,28,0xFFFFFFFF	rotrwi r6,r4,4
rlwinm r6,r4,1,0,30	rlwinm r6,r4,1,0xFFFFFFFE	slwi r6,r4,1
rlwinm r6,r4,31,1,31	rlwinm r6,r4,31,0x7FFFFFFF	srwi r6,r4,1
rlwinm r6,r4,0,1,31	rlwinm r6,r4,0,0x7FFFFFFF	clrlwi r6,r4,1
rlwinm r6,r4,0,0,7	rlwinm r6,r4,0,0xFF000000	clrrwi r6,r4,14
rlwinm r6,r4,6,6,25	rlwinm r6,r4,6,0x03FFFFC0	clrlslwi r6,r4,12,6

Done Field

When you are finished with the Invasm Options pop-up menu, use the Done key to return to the Listing menu.

3

Preprocessor Interface Hardware Reference

Preprocessor Interface Hardware Reference

This chapter contains additional reference information including the signal mapping for the E2449B PowerPC Interface Software.

Operating Characteristics

The following operating characteristics are not specifications, but are typical operating characteristics for the E2449B PowerPC Interface Software.

Table 29. Operating Characteristics

Microprocessor Compatibility	PowerPC 403GA, PowerPC 601, PowerPC 603, PowerPC 603e, PowerPC 604, and PowerPC 604e
Microprocessor Clock Speed	70 MHz for the 1670A, 1671A, and 16554 Logic Analyzers 100 MHz for the 16550, 16554/55/56, 1660, 1661, 1670D, and 1671D Logic Analyzers
Logic Analyzers Supported	1660A/AS,C/CS, 1670A/D, 16550A (two cards), 16554A/55A/56A (two or three cards), 16555D/56D (two or three cards). For the 403GA, the one-card 16550, 1661A/AS/C/CS, and 1671A/D are also supported.
Probes Required	Eight 16-channel probes are required for disassembly of PowerPC 601, 603/603e, and 604/604e. For the 403GA, five pods are required for disassembly. Additional pods are available.
Signal Line Loading	Typically 100 kOhm plus 10 pf.
Setup/Hold Requirement	Data must be valid for a 3.5 ns window with respect to the logic analyzer clock.

Signal-to-Connector Mapping

The following tables show the electrical signal-to-connector mapping required by the E2449B PowerPC Interface Software.

If you are using the 2x19 AMP Mictor connectors, you can allocate the odd and even pods at your convenience. (Note that the odd pod has even pin numbers, and the even pod has odd pin numbers.) The tables in this chapter use the convention that even-numbered pods (J2, P4, for example) use the even pod on the 2x19, and vice versa.

Table 30. PowerPC 403GA Logic Analyzer Interface Signal List - Pod J1

2x20 pin	2x10 pin	2x19 pin	LA bit	403GA pin	signal name	analyzer labels		
7	4	8	15	11	BootW	BootW		STAT
9	5	10	14	12	BusErr	BusErr		STAT
11	6	12	13	136	Error	Error		STAT
13	7	14	12	134	HoldAck	HldAck		STAT
15	8	16	11	122	WBE0 A4	WBE0	WBE0:3	STAT
17	9	18	10	123	WBE1 A5	WBE1	WBE0:3	STAT
19	10	20	9	92	A6			ADDR
21	11	22	8	93	A7			ADDR
23	12	24	7	94	A8			ADDR
25	13	26	6	95	A9			ADDR
27	14	28	5	96	A10			ADDR
29	15	30	4	97	A11			ADDR
31	16	32	3	98	A12			ADDR
33	17	34	2	99	A13			ADDR
35	18	36	1	103	A14			ADDR
37	19	38	0	104	A15			ADDR

Table 30. PowerPC 403GA Logic Analyzer Interface Signal List - Pod J2

2x20 pin	2x10 pin	2x19 pin	LA bit	403GA pin	signal name	analyzer label
7	4	7	15	105	A16	ADDR
9	5	9	14	106	A17	ADDR
11	6	11	13	107	A18	ADDR
13	7	13	12	108	A19	ADDR
15	8	15	11	109	A20	ADDR
17	9	17	10	110	A21	ADDR
19	10	19	9	112	A22	ADDR
21	11	21	8	113	A23	ADDR
23	12	23	7	114	A24	ADDR
25	13	25	6	115	A25	ADDR
27	14	27	5	116	A26	ADDR
29	15	29	4	117	A27	ADDR
31	16	31	3	118	A28	ADDR
33	17	33	2	119	A29	ADDR
35	18	35	1		gnd	ADDR
37	19	37	0		gnd	ADDR

Table 30. PowerPC 403GA Logic Analyzer Interface Signal List - Pod J3

2x20 pin	2x10 pin	2x19 pin	LA bit	403GA pin	signal name	analyzer label
7	4	8	15	42	D0	DATA
9	5	10	14	43	D1	DATA
11	6	12	13	44	D2	DATA
13	7	14	12	45	D3	DATA
15	8	16	11	46	D4	DATA
17	9	18	10	47	D5	DATA
19	10	20	9	48	D6	DATA
21	11	22	8	51	D7	DATA
23	12	24	7	52	D8	DATA
25	13	26	6	53	D9	DATA
27	14	28	5	54	D10	DATA
29	15	30	4	55	D11	DATA
31	16	32	3	56	D12	DATA
33	17	34	2	57	D13	DATA
35	18	36	1	58	D14	DATA
37	19	38	0	62	D15	DATA

Table 30. PowerPC 403GA Logic Analyzer Interface Signal List - Pod J4

2x20 pin	2x10 pin	2x19 pin	LA bit	403GA pin	signal name	analyzer label
7	4	7	15	63	D16	DATA
9	5	9	14	64	D17	DATA
11	6	11	13	65	D18	DATA
13	7	13	12	66	D19	DATA
15	8	15	11	67	D20	DATA
17	9	17	10	68	D21	DATA
19	10	19	9	71	D22	DATA
21	11	21	8	72	D23	DATA
23	12	23	7	73	D24	DATA
25	13	25	6	74	D25	DATA
27	14	27	5	75	D26	DATA
29	15	29	4	76	D27	DATA
31	16	31	3	77	D28	DATA
33	17	33	2	78	D29	DATA
35	18	35	1	79	D30	DATA
37	19	37	0	82	D31	DATA

Table 30. PowerPC 403GA Logic Analyzer Interface Signal List - Pod J5

2x20 pin	2x10 pin	2x19 pin	LA bit	403GA pin	signal name	analyzer labels		
3	3	6	clk1	22	SysCLK	C2CLK		
7	4	8	15	31	INT0	Intr 0	Intrpt	STAT
9	5	10	14	32	INT1	Intr 1	Intrpt	STAT
11	6	12	13	33	INT2	Intr 2	Intrpt	STAT
13	7	14	12	34	INT3	Intr 3	Intrpt	STAT
15	8	16	11	35	INT4	Intr 4	Intrpt	STAT
17	9	18	10	36	CINT	Crit In	Intrpt	STAT
19	10	20	9	124	WBE2 A30	WBE2	WBE0:3	STAT
21	11	22	8	125	WBE3 A31	WBE3	WBE0:3	STAT
23	12	24	7	127	R/W-	R/-W	TS0:6	STAT
25	13	26	6	17	ES0 TS0	ES0:2	TS0:6	STAT
27	14	28	5	18	ES1 TS1	ES0:2	TS0:6	STAT
29	15	30	4	19	ES2 TS2	ES0:2	TS0:6	STAT
31	16	32	3	86	BTS TS3	BTS	TS0:6	STAT
33	17	34	2	85	DMA- TS4	-DMA	TS0:6	STAT
35	18	36	1	84	I/D- TS5	I/D-	TS0:6	STAT
37	19	38	0	83	IOTV TS6	IOTV	TS0:6	STAT

Table 30. PowerPC 403GA Logic Analyzer Interface Signal List - Pod J6

2x20 pin	2x10 pin	2x19 pin	LA bit	403GA pin	signal name	analyzer labels	
7	4	7	15	14	HoldReq	Hold	
9	5	9	14	91	Reset-	Reset-	
11	6	11	13	135	BusReq	BusReq	
13	7	13	12	139	MuxSel	AmuxS	
15	8	15	11	2	Req0	-DMAR0	Req0:3
17	9	17	10	3	Req1	-DMAR1	Req0:3
19	10	19	9	4	Req2	-DMAR2	Req0:3
21	11	21	8	5	Req3	-DMAR3	Req0:3
23	12	23	7	156	Ack0	-DMAA0	Ack0:3
25	13	25	6	157	Ack1	-DMAA1	Ack0:3
27	14	27	5	158	Ack2	-DMAA2	Ack0:3
29	15	29	4	159	Ack3	-DMAA3	Ack0:3
31	16	31	3	128	EOT0	-EOT0	EOT0:3
33	17	33	2	131	EOT1	-EOT1	EOT0:3
35	18	35	1	132	EOT2	-EOT2	EOT0:3
37	19	37	0	133	EOT3	-EOT3	EOT0:3

Table 30. PowerPC 403GA Logic Analyzer Interface Signal List - Pod J7

2x20 pin	2x10 pin	2x19 pin	LA bit	403GA pin	signal name	analyzer labels		
7	4	8	15	155	CS0	CS0:7		
9	5	10	14	154	CS1	CS0:7		
11	6	12	13	153	CS2	CS0:7		
13	7	14	12	152	CS3	CS0:7		
15	8	16	11	13	Ready	Ready		
17	9	18	10	126	OE	OE		
19	10	20	9	137	DramOE	DramOE		
21	11	22	8	138	DramWE	DramWE		
23	12	24	7	145	CAS3	CAS3	CAS3:0	
25	13	26	6	144	CAS2	CAS2	CAS3:0	
27	14	28	5	143	CAS1	CAS1	CAS3:0	
29	15	30	4	142	CAS0	CAS0	CAS3:0	
31	16	32	3	151	CS4/RAS3	CS4 RAS3	CAS0:7	RAS3:0
33	17	34	2	148	CS5/RAS2	CS5 RAS2	CAS0:7	RAS3:0
35	18	36	1	147	CS6/RAS1	CS6 RAS1	CAS0:7	RAS3:0
37	19	38	0	146	CS7/RAS0	CS7 RAS0	CAS0:7	RAS3:0

Table 30. PowerPC 403GA Logic Analyzer Interface Signal List - Pod J8

2x20 pin	2x10 pin	2x19 pin	LA bit	403GA pin	signal name	analyzer label
3	3	5	clk1	6	TCK	TCLK
7	4	7	15	7	TMS	TMS
9	5	9	14	8	TDI	TDI
11	6	11	13	16	TDO	TDO
13	7	13	12	9	Halt-	Halt
15	8	15	11	26	SerClk	SerClk
17	9	17	10	27	RecvD	RecvD
19	10	19	9	87	XmitD	XmitD
21	11	21	8	88	DTR/RTS	-DTR -RTS
23	12	23	7	28	DSR/CTS	-DSR -CTS
25	13	25	6	25	Timer	TimClk
27	14	27	5	23	TestA	Test A
29	15	29	4	24	TestB	Test B
31	16	31	3	--	--	
33	17	33	2	--	--	
35	18	35	1	37	FrqR0	FreqR0
37	19	37	0	38	FrqR1	FreqR1

Table 31. PowerPC 601 Logic Analyzer Interface Signal List - Pod P1

2x20 pin	2x10 pin	2x19 pin	LA bit	601 pin	signal name	analyzer labels	
3	3	6	clk1	229	XATS	XATS-	STAT
7	4	8	15	43	A16		ADDR
9	5	10	14	45	A17		ADDR
11	6	12	13	46	A18		ADDR
13	7	14	12	47	A19		ADDR
15	8	16	11	49	A20		ADDR
17	9	18	10	50	A21		ADDR
19	10	20	9	51	A22		ADDR
21	11	22	8	54	A23		ADDR
23	12	24	7	55	A24		ADDR
25	13	26	6	56	A25		ADDR
27	14	28	5	58	A26		ADDR
29	15	30	4	59	A27		ADDR
31	16	32	3	60	A28		ADDR
33	17	34	2	62	A29		ADDR
35	18	36	1	63	A30		ADDR
37	19	38	0	64	A31		ADDR

Table 31. PowerPC 601 Logic Analyzer Interface Signal List - Pod P2

2x20 pin	2x10 pin	2x19 pin	LA bit	601 pin	signal name	analyzer labels
3	3	5	clk1	226	TS	TS-
7	4	7	15	18	A0	ADDR
9	5	9	14	19	A1	ADDR
11	6	11	13	21	A2	ADDR
13	7	13	12	22	A3	ADDR
15	8	15	11	23	A4	ADDR
17	9	17	10	26	A5	ADDR
19	10	19	9	27	A6	ADDR
21	11	21	8	28	A7	ADDR
23	12	23	7	30	A8	ADDR
25	13	25	6	31	A9	ADDR
27	14	27	5	32	A10	ADDR
29	15	29	4	34	A11	ADDR
31	16	31	3	35	A12	ADDR
33	17	33	2	36	A13	ADDR
35	18	35	1	41	A14	ADDR
37	19	37	0	42	A15	ADDR

Table 31. PowerPC 601 Logic Analyzer Interface Signal List - Pod P3

2x20 pin	2x10 pin	2x19 pin	LA bit	601 pin	signal name	analyzer labels
3	3	6	clk1	285	PCLK_EN	PCLKEN
7	4	8	15	151	DL16	DATA_B
9	5	10	14	149	DL17	DATA_B
11	6	12	13	148	DL18	DATA_B
13	7	14	12	147	DL19	DATA_B
15	8	16	11	145	DL20	DATA_B
17	9	18	10	144	DL21	DATA_B
19	10	20	9	143	DL22	DATA_B
21	11	22	8	140	DL23	DATA_B
23	12	24	7	139	DL24	DATA_B
25	13	26	6	138	DL25	DATA_B
27	14	28	5	136	DL26	DATA_B
29	15	30	4	135	DL27	DATA_B
31	16	32	3	134	DL28	DATA_B
33	17	34	2	132	DL29	DATA_B
35	18	36	1	131	DL30	DATA_B
37	19	38	0	130	DL31	DATA_B

Table 31. PowerPC 601 Logic Analyzer Interface Signal List - Pod P4

2x20 pin	2x10 pin	2x19 pin	LA bit	601 pin	signal name	analyzer labels
3	3	5	clk1	271	BCLK_EN	BCLKEN
7	4	7	15	188	DL0	DATA_B
9	5	9	14	185	DL1	DATA_B
11	6	11	13	182	DL2	DATA_B
13	7	13	12	181	DL3	DATA_B
15	8	15	11	180	DL4	DATA_B
17	9	17	10	178	DL5	DATA_B
19	10	19	9	173	DL6	DATA_B
21	11	21	8	172	DL7	DATA_B
23	12	23	7	169	DL8	DATA_B
25	13	25	6	168	DL9	DATA_B
27	14	27	5	167	DL10	DATA_B
29	15	29	4	165	DL11	DATA_B
31	16	31	3	161	DL12	DATA_B
33	17	33	2	159	DL13	DATA_B
35	18	35	1	157	DL14	DATA_B
37	19	37	0	155	DL15	DATA_B

Table 31. PowerPC 601 Logic Analyzer Interface Signal List - Pod P5

2x20 pin	2x10 pin	2x19 pin	LA bit	601 pin	signal name	analyzer label
3	3	6	clk1	--	--	
7	4	8	15	99	DH16	DATA
9	5	10	14	98	DH17	DATA
11	6	12	13	97	DH18	DATA
13	7	14	12	95	DH19	DATA
15	8	16	11	94	DH20	DATA
17	9	18	10	93	DH21	DATA
19	10	20	9	91	DH22	DATA
21	11	22	8	90	DH23	DATA
23	12	24	7	86	DH24	DATA
25	13	26	6	85	DH25	DATA
27	14	28	5	84	DH26	DATA
29	15	30	4	83	DH27	DATA
31	16	32	3	82	DH28	DATA
33	17	34	2	81	DH29	DATA
35	18	36	1	80	DH30	DATA
37	19	38	0	75	DH31	DATA

Table 31. PowerPC 601 Logic Analyzer Interface Signal List - Pod P6

2x20 pin	2x10 pin	2x19 pin	LA bit	601 pin	signal name	analyzer label
3	3	5	clk1	--	--	
7	4	7	15	127	DH0	DATA
9	5	9	14	126	DH1	DATA
11	6	11	13	125	DH2	DATA
13	7	13	12	123	DH3	DATA
15	8	15	11	122	DH4	DATA
17	9	17	10	121	DH5	DATA
19	10	19	9	119	DH6	DATA
21	11	21	8	118	DH7	DATA
23	12	23	7	112	DH8	DATA
25	13	25	6	111	DH9	DATA
27	14	27	5	110	DH10	DATA
29	15	29	4	108	DH11	DATA
31	16	31	3	107	DH12	DATA
33	17	33	2	106	DH13	DATA
35	18	35	1	104	DH14	DATA
37	19	37	0	103	DH15	DATA

Table 31. PowerPC 601 Logic Analyzer Interface Signal List - Pod P7

2x20 pin	2x10 pin	2x19 pin	LA bit	601 pin	signal name	analyzer labels		
3	3	6	clk1	--	--			
7	4	8	15	219	BR	BR-		STAT
9	5	10	14	298	BG	BG-		STAT
11	6	12	13	300	DBG	DBG-		STAT
13	7	14	12	297	DBWO	DBWO-		STAT
15	8	16	11	224	ABB	ABB-		STAT
17	9	18	10	220	DBB	DBB-		STAT
19	10	20	9	291	TEA	TEA-		STAT
21	11	22	8	262	INT	INT-		STAT
23	12	24	7	295	AACK	AACK-	AACKs	STAT
25	13	26	6	221	ARTRY	ARTRY-	AACKs	STAT
27	14	28	5	290	TA	TA-	AACKs	STAT
29	15	30	4	292	DRTRY	DRTRY-	AACKs	STAT
31	16	32	3	279	HRESET	HRESET-		
33	17	34	2	264	SRESET	SRESET-		
35	18	36	1	258	CKSTP_IN	CHKIN-		
37	19	38	0	235	SHD	SHD-		

Table 31. PowerPC 601 Logic Analyzer Interface Signal List - Pod P8

2x20 pin	2x10 pin	2x19 pin	LA bit	601 pin	signal name	analyzer label		
3	3	5	clk1	--	--			
7	4	7	15	216	CI	CI-		STAT
9	5	9	14	214	WT	WT-		STAT
11	6	11	13	233	GBL	GBL-		STAT
13	7	13	12		--			STAT
15	8	15	11	243	TC0		TC	STAT
17	9	17	10	251	TC1		TC	STAT
19	10	19	9		--			STAT
21	11	21	8	236	TBST	TBST-	TSIZ	STAT
23	12	23	7	228	TT0	Atomic	TT	STAT
25	13	25	6	227	TT1	R/-W	TT	STAT
27	14	27	5	248	TT2	Invalid	TT	STAT
29	15	29	4	244	TT3	A Only	TT	STAT
31	16	31	3	238	TT4		TT	STAT
33	17	33	2	241	TSIZ0		TSIZ	STAT
35	18	35	1	232	TSIZ1		TSIZ	STAT
37	19	37	0	237	TSIZ2		TSIZ	STAT

Table 31. PowerPC 601 Logic Analyzer Interface Signal List - Pod P9

2x20 pin	2x10 pin	2x19 pin	LA bit	601 pin	signal name	analyzer label
3	3	6	clk1	282	2X_PCLK	2XPCLK
7	4	8	15		--	
9	5	10	14		--	
11	6	12	13	231	APE	APE-
13	7	14	12	222	DPE	DPE-
15	8	16	11	67	AP0	AP
17	9	18	10	68	AP1	AP
19	10	20	9	69	AP2	AP
21	11	22	8	71	AP3	AP
23	12	24	7	203	DP0	DP
25	13	26	6	202	DP1	DP
27	14	28	5	201	DP2	DP
29	15	30	4	199	DP3	DP
31	16	32	3	198	DP4	DP
33	17	34	2	197	DP5	DP
35	18	36	1	195	DP6	DP
37	19	38	0	194	DP7	DP

Table 31. PowerPC 601 Logic Analyzer Interface Signal List - Pod P10

2x20 pin	2x10 pin	2x19 pin	LA bit	601 pin	signal name	analyzer labels	
3	3	5	clk1		--		
7	4	7	15		--		
9	5	9	14		--		
11	6	11	13		--		
13	7	13	12		--		
15	8	15	11		--		
17	9	17	10		--		
19	10	19	9		--		
21	11	21	8		--		
23	12	23	7	72	CKSTP_OUT	CHKOUT	
25	13	25	6		--		
27	14	27	5	215	CSE0		CSE
29	15	29	4	211	CSE1		CSE
31	16	31	3	212	CSE2		CSE
33	17	33	2	273	RTC	RTC	
35	18	35	1		--		
37	19	37	0	254	RSRV	RSRV-	

Table 32. PowerPC 603/603e Logic Analyzer Interface Signal List - Pod J1

2x20 pin	2x10 pin	2x19 pin	LA bit	603/603e pin	signal name	analyzer labels	
3	3	6	clk1	221	CLKOUT		CLKOUT
7	4	8	15	231	AP0	AP	
9	5	10	14	230	AP1	AP	
11	6	12	13	227	AP2	AP	
13	7	14	12	226	AP3	AP	
15	8	16	11	186	MCP		MCP-
17	9	18	10	187	SMI		SMI-
19	10	20	9	198	TDO		TDO
21	11	22	8	200	TMS		TMS
23	12	24	7	199	TDI		TDI
25	13	26	6	202	TRST		TRST-
27	14	28	5	--	--		
29	15	30	4	205	LSSDMODE		LSSDMO
31	16	32	3	213	PLLCF0	PLLCFG	
33	17	34	2	211	PLLCF1	PLLCFG	
35	18	36	1	210	PLLCF2	PLLCFG	
37	19	38	0	208	PLLCF3	PLLCFG	

Table 32. PowerPC 603/603e Logic Analyzer Interface Signal List - Pod J2

2x20 pin	2x10 pin	2x19 pin	LA bit	603/603e pin	signal name	analyzer labels		
3	3	5	clk1	235	QACK			QACK-
7	4	7	15	214	HRESET	STAT		HRESET-
9	5	9	14	215	CKSTP	STAT		CKSTP-
11	6	11	13	216	CHECK STOP	STAT		CKHOUT
13	7	13	12	219	BR	STAT		BR-
15	8	15	11	224	TC0	STAT	TC	TC0
17	9	17	10	223	TC1	STAT	TC	TC1
19	10	19	9	236	WT	STAT		WT-
21	11	21	8	237	CI	STAT		CI-
23	12	23	7	1	GBL	STAT		GBL-
25	13	25	6	25	DBWO	STAT		DBWO-
27	14	27	5	26	DBG	STAT		DBG-
29	15	29	4	27	BG	STAT		BG-
31	16	31	3	28	AACK	STAT	acks	AACK-
33	17	33	2	31	QREQ	STAT		QREQ-
35	18	35	1	32	ARTRY	STAT	acks	ARTRY-
37	19	37	0	36	ABB	STAT		ABB-

Table 32. PowerPC 603/603e Logic Analyzer Interface Signal List - Pod J3

2x20 pin	2x10 pin	2x19 pin	LA bit	603/603e pin	signal name	analyzer label
3	3	6	clk1	--		
7	4	8	15	179	A0	ADDR
9	5	10	14	2	A1	ADDR
11	6	12	13	178	A2	ADDR
13	7	14	12	3	A3	ADDR
15	8	16	11	176	A4	ADDR
17	9	18	10	5	A5	ADDR
19	10	20	9	175	A6	ADDR
21	11	22	8	6	A7	ADDR
23	12	24	7	174	A8	ADDR
25	13	26	6	7	A9	ADDR
27	14	28	5	170	A10	ADDR
29	15	30	4	11	A11	ADDR
31	16	32	3	169	A12	ADDR
33	17	34	2	12	A13	ADDR
35	18	36	1	168	A14	ADDR
37	19	38	0	13	A15	ADDR

Table 32. PowerPC 603/603e Logic Analyzer Interface Signal List - Pod J4

2x20 pin	2x10 pin	2x19 pin	LA bit	603/603e pin	signal name	analyzer label
3	3	5	clk1	212	SYSCLK	SYSCLK
7	4	7	15	166	A16	ADDR
9	5	9	14	15	A17	ADDR
11	6	11	13	169	A18	ADDR
13	7	13	12	16	A19	ADDR
15	8	15	11	164	A20	ADDR
17	9	17	10	17	A21	ADDR
19	10	19	9	160	A22	ADDR
21	11	21	8	21	A23	ADDR
23	12	23	7	157	A24	ADDR
25	13	25	6	22	A25	ADDR
27	14	27	5	158	A26	ADDR
29	15	29	4	23	A27	ADDR
31	16	31	3	151	A28	ADDR
33	17	33	2	30	A29	ADDR
35	18	35	1	144	A30	ADDR
37	19	37	0	37	A31	ADDR

Table 32. PowerPC 603/603e Logic Analyzer Interface Signal List - Pod J5

2x20 pin	2x10 pin	2x19 pin	LA bit	603/603e pin	signal name	analyzer labels		
3	3	6	clk1	180	TT4			TT4
7	4	8	15	197	TSIZ0	STAT	TSIZ	
9	5	10	14	196	TSIZ1	STAT	TSIZ	
11	6	12	13	195	TSIZ2	STAT	TSIZ	
13	7	14	12	192	TBST	STAT	TSIZ	TBST-
15	8	16	11	191	TT0	STAT	TT	Atomic
17	9	18	10	190	TT1	STAT	TT	R/W-
19	10	20	9	185	TT2	STAT	TT	Invldt
21	11	22	8	184	TT3	STAT	TT	A Only
23	12	24	7	189	SRESET	STAT		SRESET-
25	13	26	6	188	INT	STAT		INT-
27	14	28	5	156	DRTRY	STAT	ACKs	DRTRY
29	15	30	4	155	TA	STAT	ACKs	TA-
31	16	32	3	154	TEA	STAT	ACKs	TEA-
33	17	34	2	150	XATS*	STAT		XATS-*
35	18	36	1	149	TS	STAT		TS-
37	19	38	0	145	DBB	STAT		DBB-

*If you are probing a 603e, the signal labeled XATS- is actually CSE1 (and CSE, on pod J6, is actually CSE0). You may wish to change the name of this label. In the format menu, select the XATS label, and use the Modify Label feature to change the name to CSE1. (DO NOT modify the bit assignments to the STAT label.)

Table 32. PowerPC 603/603e Logic Analyzer Interface Signal List - Pod J6

2x20 pin	2x10 pin	2x19 pin	LA bit	603/603e pin	signal name	analyzer labels	
3	3	5	clk1	201	TCK		TCK
7	4	7	15	204	L1TSTCLK		L1Tclk
9	5	9	14	203	L2TSTCLK		L2Tclk
11	6	11	13	218	APE		APE
13	7	13	12	217	DPE		DPE
15	8	15	11	225	CSE		CSE
17	9	17	10	232	RSRV		RSRV-
19	10	19	9	234	TBEN		TBEN
21	11	21	8	233	TBLISYNC		TBLISY
23	12	23	7	38	DP0	DP	
25	13	25	6	40	DP1	DP	
27	14	27	5	41	DP2	DP	
29	15	29	4	42	DP3	DP	
31	16	31	3	46	DP4	DP	
33	17	33	2	47	DP5	DP	
35	18	35	1	48	DP6	DP	
37	19	37	0	50	DP7	DP	

Table 32. PowerPC 603/603e Logic Analyzer Interface Signal List - Pod J7

2x20 pin	2x10 pin	2x19 pin	LA bit	603/603e pin	signal name	analyzer label
3	3	6	clk1			
7	4	8	15	85	DH16	DATA
9	5	10	14	84	DH17	DATA
11	6	12	13	83	DH18	DATA
13	7	14	12	82	DH19	DATA
15	8	16	11	81	DH20	DATA
17	9	18	10	80	DH21	DATA
19	10	20	9	78	DH22	DATA
21	11	22	8	76	DH23	DATA
23	12	24	7	75	DH24	DATA
25	13	26	6	74	DH25	DATA
27	14	28	5	73	DH26	DATA
29	15	30	4	72	DH27	DATA
31	16	32	3	71	DH28	DATA
33	17	34	2	68	DH29	DATA
35	18	36	1	67	DH30	DATA
37	19	38	0	66	DH31	DATA

Table 32. PowerPC 603/603e Logic Analyzer Interface Signal List - Pod J8

2x20 pin	2x10 pin	2x19 pin	LA bit	603/603e pin	signal name	analyzer label
3	3	5	clk1	--		
7	4	7	15	117	DL16	DATA_B
9	5	9	14	107	DL17	DATA_B
11	6	11	13	106	DL18	DATA_B
13	7	13	12	105	DL19	DATA_B
15	8	15	11	102	DL20	DATA_B
17	9	17	10	101	DL21	DATA_B
19	10	19	9	100	DL22	DATA_B
21	11	21	8	51	DL23	DATA_B
23	12	23	7	52	DL24	DATA_B
25	13	25	6	55	DL25	DATA_B
27	14	27	5	56	DL26	DATA_B
29	15	29	4	57	DL27	DATA_B
31	16	31	3	58	DL28	DATA_B
33	17	33	2	62	DL29	DATA_B
35	18	35	1	63	DL30	DATA_B
37	19	37	0	64	DL31	DATA_B

Table 32. PowerPC 603/603e Logic Analyzer Interface Signal List - Pod J9

2x20 pin	2x10 pin	2x19 pin	LA bit	603/603e pin	signal name	analyzer label
3	3	6	clk1	--		
7	4	8	15	115	DH0	DATA
9	5	10	14	114	DH1	DATA
11	6	12	13	113	DH2	DATA
13	7	14	12	110	DH3	DATA
15	8	16	11	109	DH4	DATA
17	9	18	10	108	DH5	DATA
19	10	20	9	99	DH6	DATA
21	11	22	8	98	DH7	DATA
23	12	24	7	97	DH8	DATA
25	13	26	6	94	DH9	DATA
27	14	28	5	93	DH10	DATA
29	15	30	4	92	DH11	DATA
31	16	32	3	91	DH12	DATA
33	17	34	2	90	DH13	DATA
35	18	36	1	89	DH14	DATA
37	19	38	0	87	DH15	DATA

Table 32. PowerPC 603/603e Logic Analyzer Interface Signal List - Pod J10

2x20 pin	2x10 pin	2x19 pin	LA bit	603/603e pin	signal name	analyzer label
3	3	5	clk1	153	DBDIS	DBDIS-
7	4	7	15	143	DL0	DATA_B
9	5	9	14	141	DL1	DATA_B
11	6	11	13	140	DL2	DATA_B
13	7	13	12	139	DL3	DATA_B
15	8	15	11	135	DL4	DATA_B
17	9	17	10	134	DL5	DATA_B
19	10	19	9	133	DL6	DATA_B
21	11	21	8	131	DL7	DATA_B
23	12	23	7	130	DL8	DATA_B
25	13	25	6	129	DL9	DATA_B
27	14	27	5	126	DL10	DATA_B
29	15	29	4	125	DL11	DATA_B
31	16	31	3	124	DL12	DATA_B
33	17	33	2	123	DL13	DATA_B
35	18	35	1	119	DL14	DATA_B
37	19	37	0	118	DL15	DATA_B

Table 33. PowerPC 604/604e Logic Analyzer Interface Signal List

Pod / Connector	2x20 pin	2x10 pin	2x19 pin	Analyzer Bit	PDS Pin #	Signal Name	Analyzer Label	Analyzer Label
P4/J2even	3	3	5	CLK1	--			
P4/J2even	7	4	7	15	1	A0	ADDR	
P4/J2even	9	5	9	14	2	A1	ADDR	
P4/J2even	11	6	11	13	3	A2	ADDR	
P4/J2even	13	7	13	12	4	A3	ADDR	
P4/J2even	15	8	15	11	5	A4	ADDR	
P4/J2even	17	9	17	10	6	A5	ADDR	
P4/J2even	19	10	19	9	7	A6	ADDR	
P4/J2even	21	11	21	8	8	A7	ADDR	
P4/J2even	23	12	23	7	9	A8	ADDR	
P4/J2even	25	13	25	6	10	A9	ADDR	
P4/J2even	27	14	27	5	11	A10	ADDR	
P4/J2even	29	15	29	4	12	A11	ADDR	
P4/J2even	31	16	31	3	13	A12	ADDR	
P4/J2even	33	17	33	2	14	A13	ADDR	
P4/J2even	35	18	35	1	15	A14	ADDR	
P4/J2even	37	19	37	0	16	A15	ADDR	
P3/J2odd	3	3	6	CLK1	111	PDSCLK4	SYSCLK	
P3/J2odd	7	4	8	15	17	A16	ADDR	
P3/J2odd	9	5	10	14	18	A17	ADDR	
P3/J2odd	11	6	12	13	19	A18	ADDR	
P3/J2odd	13	7	14	12	20	A19	ADDR	
P3/J2odd	15	8	16	11	21	A20	ADDR	
P3/J2odd	17	9	18	10	22	A21	ADDR	
P3/J2odd	19	10	20	9	23	A22	ADDR	
P3/J2odd	21	11	22	8	24	A23	ADDR	
P3/J2odd	23	12	24	7	25	A24	ADDR	
P3/J2odd	25	13	26	6	26	A25	ADDR	
P3/J2odd	27	14	28	5	27	A26	ADDR	
P3/J2odd	29	15	30	4	28	A27	ADDR	
P3/J2odd	31	16	32	3	29	A28	ADDR	
P3/J2odd	33	17	34	2	30	A29	ADDR	
P3/J2odd	35	18	36	1	31	A30	ADDR	
P3/J2odd	37	19	38	0	32	A31	ADDR	

Table 33. PowerPC 604/604e Logic Analyzer Interface Signal List

Pod / Connector	2x20 pin	2x10 pin	2x19 pin	Analyzer Bit	PDS Pin #	Signal Name	Analyzer Label	Analyzer Label
P10/J5even	3	3	5	CLK1	--			
P10/J5even	7	4	7	15	39	DH0	DATA	
P10/J5even	9	5	9	14	40	DH1	DATA	
P10/J5even	11	6	11	13	41	DH2	DATA	
P10/J5even	13	7	13	12	42	DH3	DATA	
P10/J5even	15	8	15	11	43	DH4	DATA	
P10/J5even	17	9	17	10	44	DH5	DATA	
P10/J5even	19	10	19	9	45	DH6	DATA	
P10/J5even	21	11	21	8	46	DH7	DATA	
P10/J5even	23	12	23	7	47	DH8	DATA	
P10/J5even	25	13	25	6	48	DH9	DATA	
P10/J5even	27	14	27	5	49	DH10	DATA	
P10/J5even	29	15	29	4	50	DH11	DATA	
P10/J5even	31	16	31	3	51	DH12	DATA	
P10/J5even	33	17	33	2	52	DH13	DATA	
P10/J5even	35	18	35	1	53	DH14	DATA	
P10/J5even	37	19	37	0	54	DH15	DATA	
P8/J4even	3	3	5	CLK1				
P8/J4even	7	4	7	15	55	DH16	DATA	
P8/J4even	9	5	9	14	56	DH17	DATA	
P8/J4even	11	6	11	13	57	DH18	DATA	
P8/J4even	13	7	13	12	58	DH19	DATA	
P8/J4even	15	8	15	11	59	DH20	DATA	
P8/J4even	17	9	17	10	60	DH21	DATA	
P8/J4even	19	10	19	9	61	DH22	DATA	
P8/J4even	21	11	21	8	62	DH23	DATA	
P8/J4even	23	12	23	7	63	DH24	DATA	
P8/J4even	25	13	25	6	64	DH25	DATA	
P8/J4even	27	14	27	5	65	DH26	DATA	
P8/J4even	29	15	29	4	66	DH27	DATA	
P8/J4even	31	16	31	3	67	DH28	DATA	
P8/J4even	33	17	33	2	68	DH29	DATA	
P8/J4even	35	18	35	1	69	DH30	DATA	
P8/J4even	37	19	37	0	70	DH31	DATA	

Table 33. PowerPC 604/604e Logic Analyzer Interface Signal List

Pod / Connector	2x20 pin	2x10 pin	2x19 pin	Analyzer Bit	PDS Pin #	Signal Name	Analyzer Label	Analyzer Label
P9/J5odd	3	3	6	CLK1	114	DBDIS	DBDIS	
P9/J5odd	7	4	8	15	71	DL0	DATA_B	
P9/J5odd	9	5	10	14	72	DL1	DATA_B	
P9/J5odd	11	6	12	13	73	DL2	DATA_B	
P9/J5odd	13	7	14	12	74	DL3	DATA_B	
P9/J5odd	15	8	16	11	75	DL4	DATA_B	
P9/J5odd	17	9	18	10	76	DL5	DATA_B	
P9/J5odd	19	10	20	9	77	DL6	DATA_B	
P9/J5odd	21	11	22	8	78	DL7	DATA_B	
P9/J5odd	23	12	24	7	79	DL8	DATA_B	
P9/J5odd	25	13	26	6	80	DL9	DATA_B	
P9/J5odd	27	14	28	5	81	DL10	DATA_B	
P9/J5odd	29	15	30	4	82	DL11	DATA_B	
P9/J5odd	31	16	32	3	83	DL12	DATA_B	
P9/J5odd	33	17	34	2	84	DL13	DATA_B	
P9/J5odd	35	18	36	1	85	DL14	DATA_B	
P9/J5odd	37	19	38	0	86	DL15	DATA_B	
P7/J4odd	3	3	6	CLK1				
P7/J4odd	7	4	8	15	87	DL16	DATA_B	
P7/J4odd	9	5	10	14	88	DL17	DATA_B	
P7/J4odd	11	6	12	13	89	DL18	DATA_B	
P7/J4odd	13	7	14	12	90	DL19	DATA_B	
P7/J4odd	15	8	16	11	91	DL20	DATA_B	
P7/J4odd	17	9	18	10	92	DL21	DATA_B	
P7/J4odd	19	10	20	9	93	DL22	DATA_B	
P7/J4odd	21	11	22	8	94	DL23	DATA_B	
P7/J4odd	23	12	24	7	95	DL24	DATA_B	
P7/J4odd	25	13	26	6	96	DL25	DATA_B	
P7/J4odd	27	14	28	5	97	DL26	DATA_B	
P7/J4odd	29	15	30	4	98	DL27	DATA_B	
P7/J4odd	31	16	32	3	99	DL28	DATA_B	
P7/J4odd	33	17	34	2	100	DL29	DATA_B	
P7/J4odd	35	18	36	1	101	DL30	DATA_B	
P7/J4odd	37	19	38	0	102	DL31	DATA_B	

Table 33. PowerPC 604/604e Logic Analyzer Interface Signal List

Pod / Connector	2x20 pin	2x10 pin	2x19 pin	Analyzer Bit	PDS Pin #	Signal Name	Analyzer Label		Analyzer Label
P5/J3odd	3	3	6	CLK1					
P5/J3odd	7	4	8	15	116	TSIZ0	TSIZ		STAT
P5/J3odd	9	5	10	14	118	TSIZ1	TSIZ		STAT
P5/J3odd	11	6	12	13	120	TSIZ2	TSIZ		STAT
P5/J3odd	13	7	14	12	138	TBST	TSIZ	TBST	STAT
P5/J3odd	15	8	16	11	115	TT0	Atomic	TT	STAT
P5/J3odd	17	9	18	10	117	TT1	R/-W	TT	STAT
P5/J3odd	19	10	20	9	119	TT2	Invldt	TT	STAT
P5/J3odd	21	11	22	8	121	TT3	A Only	TT	STAT
P5/J3odd	23	12	24	7	123	TT4	TT4	TT	STAT
P5/J3odd	25	13	26	6	154	INT	INT		STAT
P5/J3odd	27	14	28	5	137	DRTRY	DRTRY	acks	STAT
P5/J3odd	29	15	30	4	139	TA	TA	acks	STAT
P5/J3odd	31	16	32	3	141	TEA	TEA		STAT
P5/J3odd	33	17	34	2	136	XATS	XATS		STAT
P5/J3odd	35	18	36	1	134	TS	TS		STAT
P5/J3odd	37	19	38	0	146	DBB	DBB		STAT
P2/J1even	3	3	5	CLK1	180	QACK	QACK		
P2/J1even	7	4	7	15	181	HRESET	HRSET		STAT
P2/J1even	9	5	9	14	160	CKSTPI	CKSTP		STAT
P2/J1even	11	6	11	13	162	CKSTPO	CHKOUT		STAT
P2/J1even	13	7	13	12	152	BR	BR		STAT
P2/J1even	15	8	15	11	122	TC0	TC0	TC	STAT
P2/J1even	17	9	17	10	124	TC1	TC1	TC	STAT
P2/J1even	19	10	19	9	126	TC2	TC2	TC	STAT
P2/J1even	21	11	21	8	127	WT	WT		STAT
P2/J1even	23	12	23	7	125	CI	CI		STAT
P2/J1even	25	13	25	6	129	GBL	GBL		STAT
P2/J1even	27	14	27	5	132	DBWO	DBWO		STAT
P2/J1even	29	15	29	4	144	DBG	DBG		STAT
P2/J1even	31	16	31	3	150	BG	BG		STAT
P2/J1even	33	17	33	2	133	AACK	AACK	acks	STAT
P2/J1even	35	18	35	1	178	QREQ	QREQ		STAT
P2/J1even	37	19	37	0	135	ARTRY	ARTRY	acks	STAT

Table 33. PowerPC 604/604e Logic Analyzer Interface Signal List

Pod / Connector	2x20 pin	2x10 pin	2x19 pin	Analyzer Bit	PDS Pin #	Signal Name	Analyzer Label	Analyzer Label
P1/J1odd	3	3	6	CLK1	186	TCK	TCK	
P1/J1odd	7	4	8	15	148	ABB	ABB	
P1/J1odd	9	5	10	14	33	AP0	AP	
P1/J1odd	11	6	12	13	34	AP1	AP	
P1/J1odd	13	7	14	12	35	AP2	AP	
P1/J1odd	15	8	16	11	36	AP3	AP	
P1/J1odd	17	9	18	10	156	MCP	MCP	
P1/J1odd	19	10	20	9	158	SMI	SMI	
P1/J1odd	21	11	22	8	182	TDO	TDO	
P1/J1odd	23	12	24	7	188	TMS	TMS	
P1/J1odd	25	13	26	6	184	TDI	TDI	
P1/J1odd	27	14	28	5	190	TRST	TRST	
P1/J1odd	29	15	30	4	164	HALTED	HALTED	
P1/J1odd	31	16	32	3	131	SHD	SHD	
P1/J1odd	33	17	34	2	176	NAPRUN	NAPRUN	
P1/J1odd	35	18	36	1	172	DRVMOD0	DRVMD0	
P1/J1odd	37	19	38	0	174	DRVMOD1	DRVMD1	
P6/J3even	3	3	5	CLK1				
P6/J3even	7	4	7	15	128	CSE0	CSE0	
P6/J3even	9	5	9	14	130	CSE1	CSE1	
P6/J3even	11	6	11	13	35	APE	APE	
P6/J3even	13	7	13	12	113	DPE	DPE	
P6/J3even	15	8	15	11	179	SRESET	SRESET	
P6/J3even	17	9	17	10	38	RSRV	RSRV	
P6/J3even	19	10	19	9	168	TBEN	TBEN	
P6/J3even	21	11	21	8	166	TLBISYNC	TLBISY	
P6/J3even	23	12	23	7	103	DP0	DP	
P6/J3even	25	13	25	6	104	DP1	DP	
P6/J3even	27	14	27	5	105	DP2	DP	
P6/J3even	29	15	29	4	106	DP3	DP	
P6/J3even	31	16	31	3	107	DP4	DP	
P6/J3even	33	17	33	2	108	DP5	DP	
P6/J3even	35	18	35	1	109	DP6	DP	
P6/J3even	37	19	37	0	110	DP7	DP	

Table 33. PowerPC 604/604e Logic Analyzer Interface Signal List

Pod / Connector	2x20 pin	2x10 pin	2x19 pin	Analyzer Bit	PDS Pin #	Signal Name	Analyzer Label	Analyzer Label
P11/J6odd	3	3	6	CLK1				
P11/J6odd	7	4	8	15	151	CACHESIZ0	C_SIZ0	CachSz
P11/J6odd	9	5	10	14	177	CACHESIZ1	C_SIZ1	CachSz
P11/J6odd	11	6	12	13	153	L2ADSC	ADSC	
P11/J6odd	13	7	14	12	155	L2BAA	BAA	
P11/J6odd	15	8	16	11	157	CACHEBR	CACHBR	
P11/J6odd	17	9	18	10	159	CACHEBG	CACHBG	
P11/J6odd	19	10	20	9	161	L2DOE	DOE	
P11/J6odd	21	11	22	8	163	L2DWE	DWE	
P11/J6odd	23	12	24	7	165	L2HIT	HIT	
P11/J6odd	25	13	26	6	167	L2TALE	TALE	
P11/J6odd	27	14	28	5	169	L2TALOE	TALOE	
P11/J6odd	29	15	30	4	170	SUSPEND	SUSPND	
P11/J6odd	31	16	32	3	171	L2TOE	TOE	
P11/J6odd	33	17	34	2	173	L2TWE	TWE	
P11/J6odd	35	18	36	1	175	L2TV	TV	
P11/J6odd	37	19	38	0	--			

A

If You Have a Problem

If You Have a Problem

Occasionally, a measurement may not give the expected results. If you encounter difficulties while making measurements, use this chapter to guide you through some possible solutions. Each heading lists a problem you may encounter, along with some possible solutions.

If you still have difficulty using the analyzer after trying the suggestions in this chapter, please contact your local Agilent service center.

CAUTION

When you are working with the analyzer, be sure to power down both the analyzer and the target system before disconnecting or connecting cables, probes, and preprocessors. Otherwise, you may damage circuitry in the analyzer, preprocessor, or target system.

Analyzer Problems

This section lists general problems that you might encounter while using the analyzer.

Intermittent data errors

This problem is usually caused by poor connections, incorrect signal levels, or marginal timing.

- ☐ **Remove and reseat all cables and probes, ensuring that there are no bent pins on the preprocessor interface or poor probe connections.**
- ☐ **Adjust the threshold level of the data pod to match the logic levels in the system under test.**
- ☐ **Use an oscilloscope to check the signal integrity of the data lines.**

  Clock signals for the state analyzer must meet particular pulse shape and timing requirements. Data inputs for the analyzer must meet pulse shape and setup and hold time requirements.

See Also See "Capacitive Loading" in this chapter for information on other sources of intermittent data errors.

Unwanted triggers

Unwanted triggers can be caused by instructions that were fetched but not executed.

- ☐ **Add the prefetch queue or pipeline depth to the trigger address to avoid this problem.**

The logic analyzer captures prefetches, even if they are not executed. When you are specifying a trigger condition or a storage qualification that follows an instruction that may cause branching, an unused prefetch may generate an unwanted trigger.

No activity on activity indicators

- ☐ Check for loose cables, board connections, and preprocessor interface connections.
- ☐ Check for bent or damaged pins on the preprocessor probe.

No trace list display

If there is no trace list display, it may be that your analysis specification is not correct for the data you want to capture, or that the trace memory is only partially filled.

- ☐ Check your analysis sequencer specification to ensure that it will capture the events of interest.
- ☐ Try stopping the analyzer; if the trace list is partially filled, this should display the contents of trace memory.

Target System Problems

This section lists problems that you might encounter with the target system. If the solutions suggested here do not correct the problem, you may have a damaged preprocessor. Contact your local Agilent Sales Office if you need further assistance.

Target system will not boot up

If the target system will not boot up after connecting the logic analyzer, the microprocessor (if socketed) or the cables may not be installed properly, or they may not be making electrical contact.

- ☐ **Ensure that you are following the correct power-on sequence for the logic analyzer and target system.**

  1 Power up the analyzer.

  2 Power up the target system.

  If you power up the target system before you power up the logic analyzer, interface circuitry may latch up and prevent proper target system operation.

- ☐ **Verify that the microprocessor and the cables are securely inserted into their respective sockets.**

- ☐ **Verify that the logic analyzer cables are in the proper sockets of the target system and are firmly inserted.**

Erratic trace measurements

There are several general problems that can cause erratic variations in trace lists and inverse assembly failures.

- ☐ **Do a full reset of the target system before beginning the measurement.**

  Some designs require a full reset to ensure correct configuration.

- ☐ **Ensure that your target system meets the timing requirements with the logic analyzer probe connected.**

  See “Capacitive Loading” in this chapter. While logic analyzer loading is slight, pin protectors, extenders, and adapters may increase it to unacceptable levels. If the target system design has close timing margins, such loading may cause incorrect processor functioning and give erratic trace results.

- ☐ **Ensure that you have sufficient cooling for the microprocessor.**

  Microprocessors such as the i486, Pentium™, and MC68040 generate substantial heat. You should ensure that you have ambient temperature conditions and airflow that meet or exceed the requirements of the microprocessor manufacturer.

Capacitive loading

Excessive capacitive loading can degrade signals, resulting in incorrect capture by the logic analyzer, or system lockup in the microprocessor. All interfaces add additional capacitive loading, as can custom probe fixtures you design for your application.

Careful layout of your target system can minimize loading problems and result in better margins for your design. This is especially important for systems that are running at frequencies greater than 50 MHz.

- ☐ **Remove as many pin protectors, extenders, and adapters as possible.**

Inverse Assembler Problems

This section lists problems that you might encounter while using the inverse assembler.

When you obtain incorrect inverse assembly results, it may be unclear whether the problem is in the preprocessor or in your target system. If you follow the suggestions in this section to ensure that you are using the preprocessor and inverse assembler correctly, you can proceed with confidence in debugging your target system.

No inverse assembly or incorrect inverse assembly

This problem may be due to incorrect synchronization, modified configuration, incorrect connections, or a hardware problem in the target system. A locked status line can cause incorrect or incomplete inverse assembly.

- ☐ **Verify that the inverse assembler has been synchronized by placing an opcode at the top of the display (not at the cursor position) and pressing the Invasm key.**

  The inverse assembler works from the first line of the trace *display.* If you jump to the middle of a trace and select Invasm, prior trace states may not be disassembled correctly. If you move to several random places in the trace list and synchronize the disassembly each time, the trace disassembly is only guaranteed to be correct for the portion of the trace list disassembled. See "To synchronize the inverse assembler" in Chapter 2 for more information.

- ☐ **Ensure that each logic analyzer pod is connected to the correct connector.**

  There is not always a one-to-one correspondence between analyzer pod numbers and connector numbers. Target systems must supply address (ADDR), data (DATA), and status (STAT) information to the analyzer in a predefined order. The cable connections for each connector are often altered to support that need. Thus, one target system might require that you connect cable 2 to analyzer pod 2, while another will require you to connect cable 5 to analyzer pod 2. See Chapter 1 for connection information.

- ☐ Check the activity indicators for status lines locked in a high or low state.
- ☐ Verify that the STAT, DATA, and ADDR format labels have not been modified from their default values.

  These labels must remain as they are configured by the configuration file. Do not change the names of these labels or the bit assignments within the labels. Some preprocessors also require other data labels. See Chapter 2 for more information.
- ☐ Verify that all microprocessor caches and memory managers have been disabled.

  In most cases, if the microprocessor caches and memory managers remain enabled you should still get inverse assembly. It may be incorrect because a portion of the execution trace was not visible to the logic analyzer.
- ☐ Verify that storage qualification has not excluded storage of all the needed opcodes and operands.

Inverse assembler will not load or run

You need to ensure that you have the correct system software loaded on your analyzer.

- ☐ Ensure that the inverse assembler is on the same disk as the configuration files you are loading.

  Configuration files for the state analyzer contain a pointer to the name of the corresponding inverse assembler. If you delete the inverse assembler or rename it, the configuration process will fail to load the disassembler.

  See Chapter 1 for details.

Intermodule Measurement Problems

Some problems occur only when you are trying to make a measurement involving multiple modules.

An event wasn't captured by one of the modules

If you are trying to capture an event that occurs very shortly after the event that arms one of the measurement modules, it may be missed due to internal analyzer delays. For example, suppose you set the oscilloscope to trigger upon receiving a trigger signal from the logic analyzer because you are trying to capture a pulse that occurs right after the analyzer's trigger state. If the pulse occurs too soon after the analyzer's trigger state, the oscilloscope will miss the pulse.

- ☐ **Adjust the skew in the Intermodule menu.**

  You may be able to specify a skew value that enables the event to be captured.

- ☐ **Change the trigger specification for modules upstream of the one with the problem.**

  If you are using a logic analyzer to trigger the scope, try specifying a trigger state one state before the one you are using. This may be more difficult than working with the skew because the prior state may occur more often and not always be related to the event you are trying to capture with the oscilloscope.

Messages

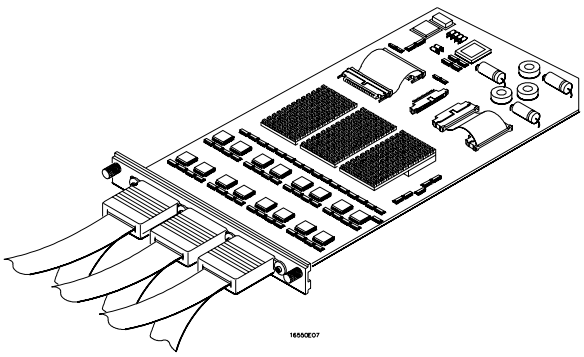
This section lists some of the messages that the analyzer displays when it encounters a problem.

". . . Inverse Assembler Not Found"

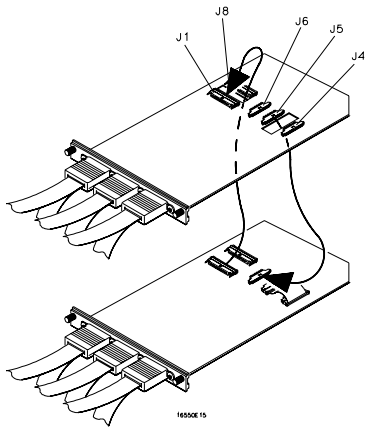
This error occurs if you rename or delete the inverse assembler file that is attached to the configuration file. Ensure that the inverse assembler file is not renamed or deleted.

"Measurement Initialization Error"

This error occurs when you have installed the cables incorrectly for one or two 16550A logic analysis cards. The following diagrams show the correct cable connections for one-card and two-card installations. Ensure that your cable connections match the silk screening on the card. Then, repeat the measurement.



Cable Connections for One-Card 16550A Installations



Cable Connections for Two-Card 16550A Installations

See Also

The *16550A 100-MHz State/500-MHz Timing Logic Analyzer Service Guide*.

"No Configuration File Loaded"

This is usually caused by trying to load a configuration file for one type of module/system into a different type of module/system.

- ☐ Verify that the appropriate module has been selected from the Load {module} from File {filename} in the 16500A/B/C disk operation menu. Selecting Load {All} will cause incorrect operation when loading most preprocessor interface configuration files.

See Also Chapter 1 describes how to load configuration files.

"Selected File is Incompatible"

This occurs when you try to load a configuration file for the wrong module. Ensure that you are loading the appropriate configuration file for your logic analyzer.

"Slow or Missing Clock"

- ☐ This error message might occur if the logic analyzer cards are not firmly seated in the 16500A/B/C or 16501A frame. Ensure that the cards are firmly seated.
- ☐ This error might occur if the target system is not running properly. Ensure that the target system is on and operating properly.
- ☐ If the error message persists, check that the logic analyzer pods are connected to the proper connectors on the preprocessor interface. See Chapter 1 to determine the proper connections.

"Waiting for Trigger"

If a trigger pattern is specified, this message indicates that the specified trigger pattern has not occurred. Verify that the triggering pattern is correctly set.

- When analyzing microprocessors that fetch only from word-aligned addresses, if the trigger condition is set to look for an opcode fetch at an address not corresponding to a word boundary, the trigger will never be found.

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About this edition

This is the first edition of the *Agilent E2449B PowerPC Software Inteface User's Guide.*

Publication number
E2449-97002, February 2002
Printed in Malaysia

Printed in USA.
E2449-97001, January 1997

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